

FIG. 1

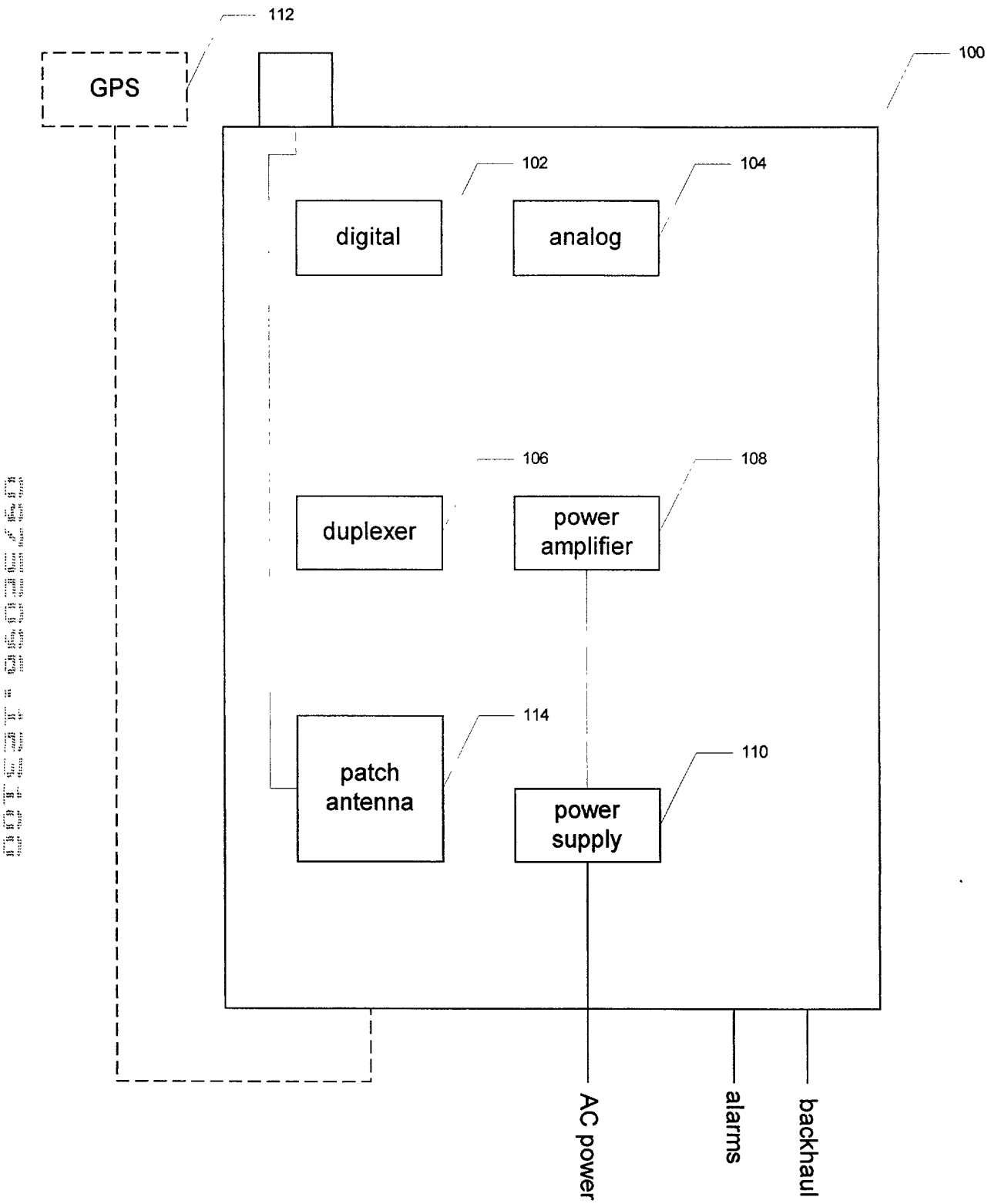


FIG. 2

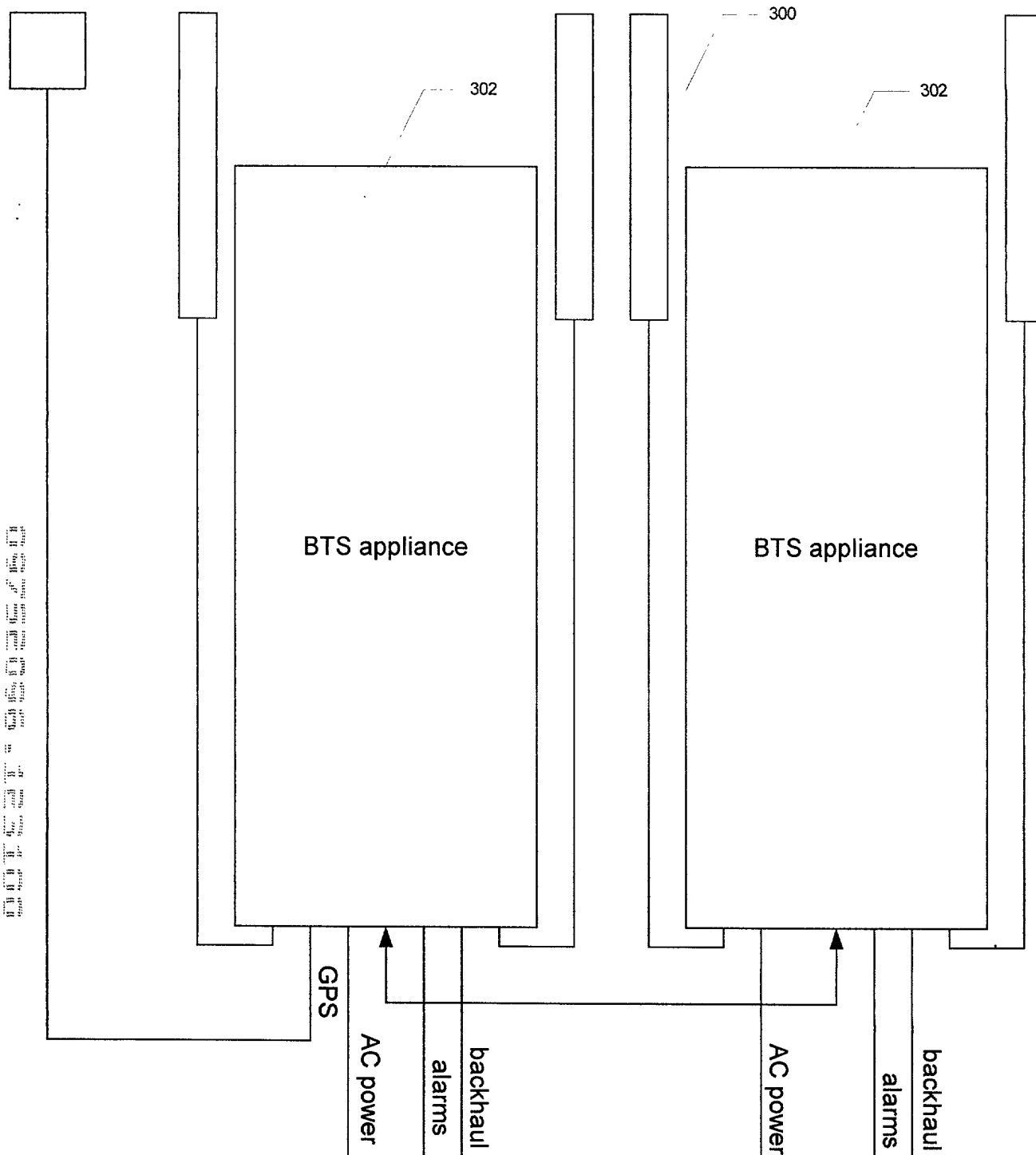


FIG. 3

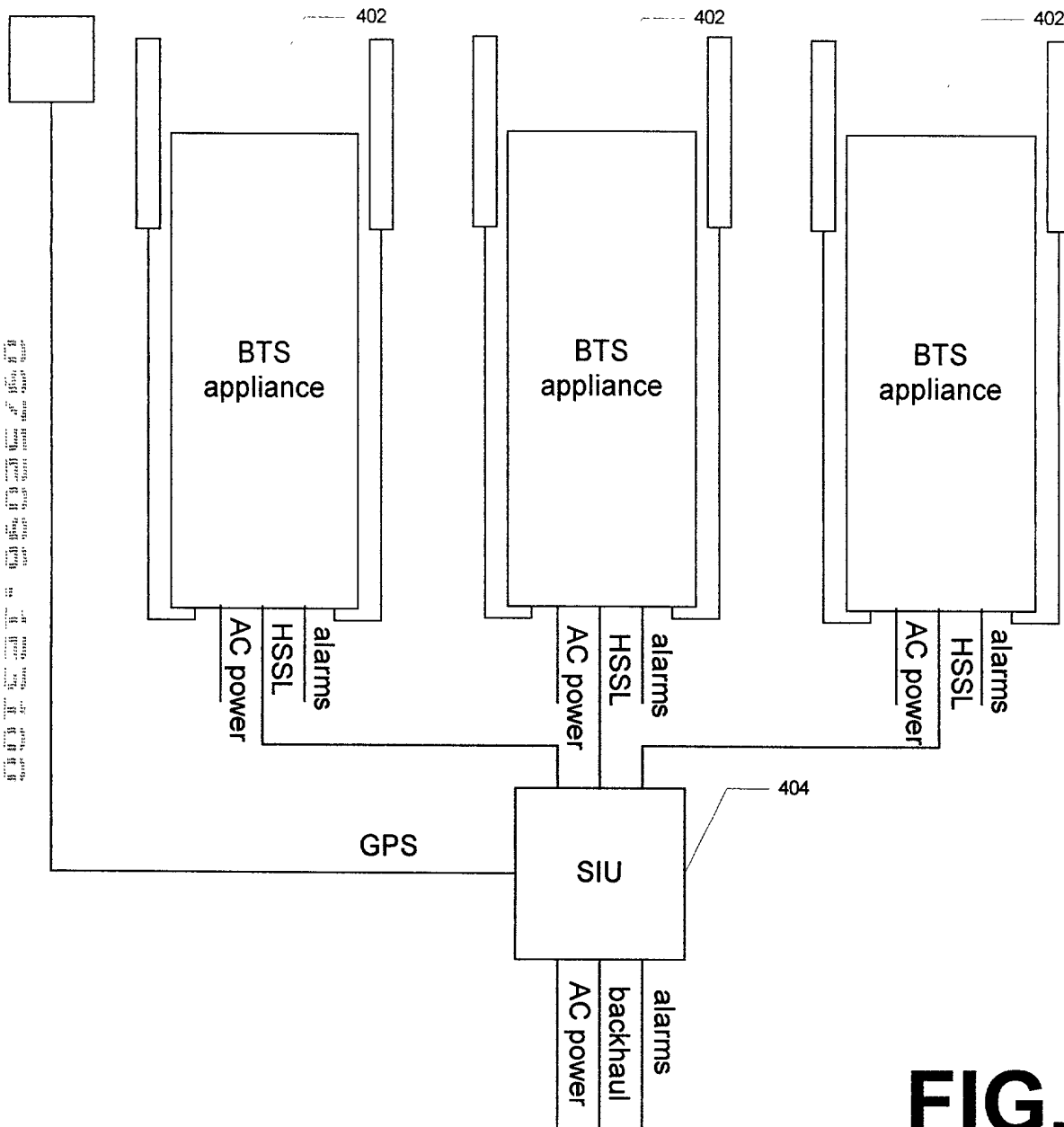
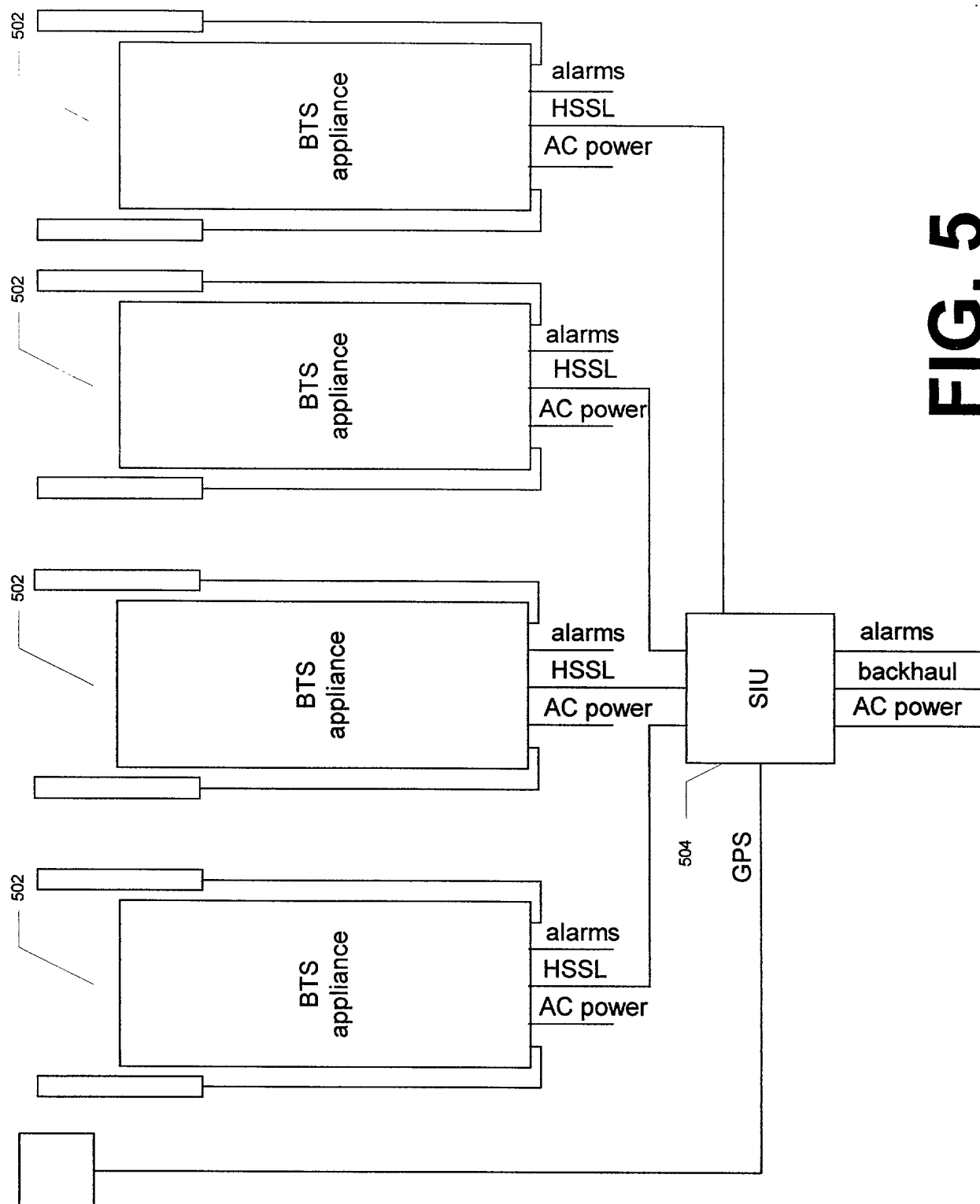


FIG. 4



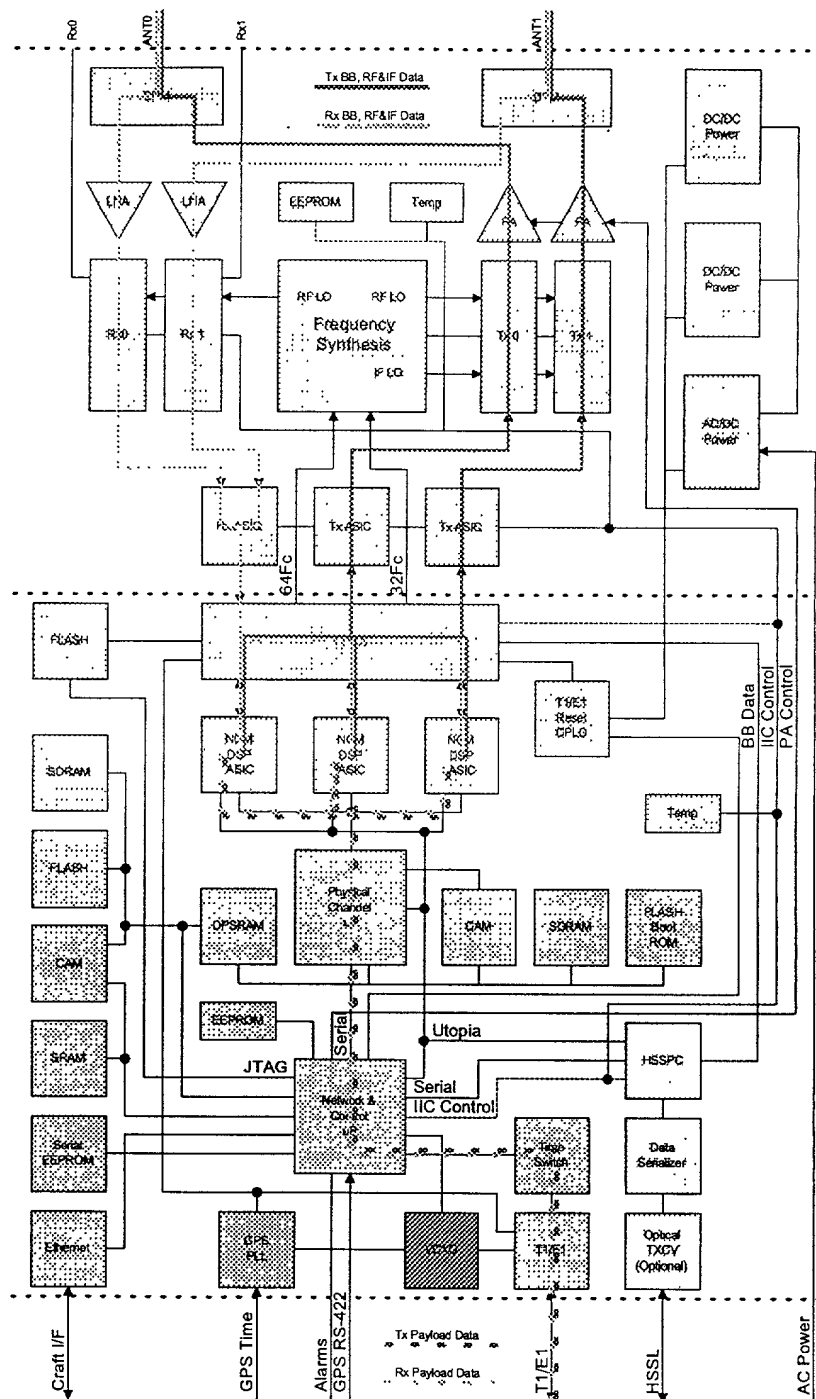


FIG. 7

FIG. 8 is a block diagram of a system 800. The system 800 includes a power supply module 802, an analog board 808, a digital board 806, a GPS module 804, and two transceiver modules 810. The power supply module 802 provides AC power and -48 V power to the system. It also provides DC power to the analog board 808 and the digital board 806. The DC power provided to the analog board 808 includes +28 V, +5 V, +5 V, +3.3 V, and +2.5 V. The DC power provided to the digital board 806 includes +3.3 V and +2.5 V. The power supply module 802 also provides a fault signal and an IIC signal to the digital board 806. The analog board 808 includes two 5W PA modules (Tx1 and Tx0) and two duplexers (Rx1 and Rx0). The digital board 806 includes an RS-485 interface, a control interface, a 64Fc interface, a 32Fc interface, a Tx1 interface, a Tx0 interface, and an Rx0&1 interface. The GPS module 804 provides a GPS signal and GPS time to the digital board 806. The digital board 806 also provides power to the GPS module 804. The digital board 806 also provides HSSL, backhaul, alarms, craft I/F, fan control, and power to the system. The transceiver modules 810 provide RF signals to the system.

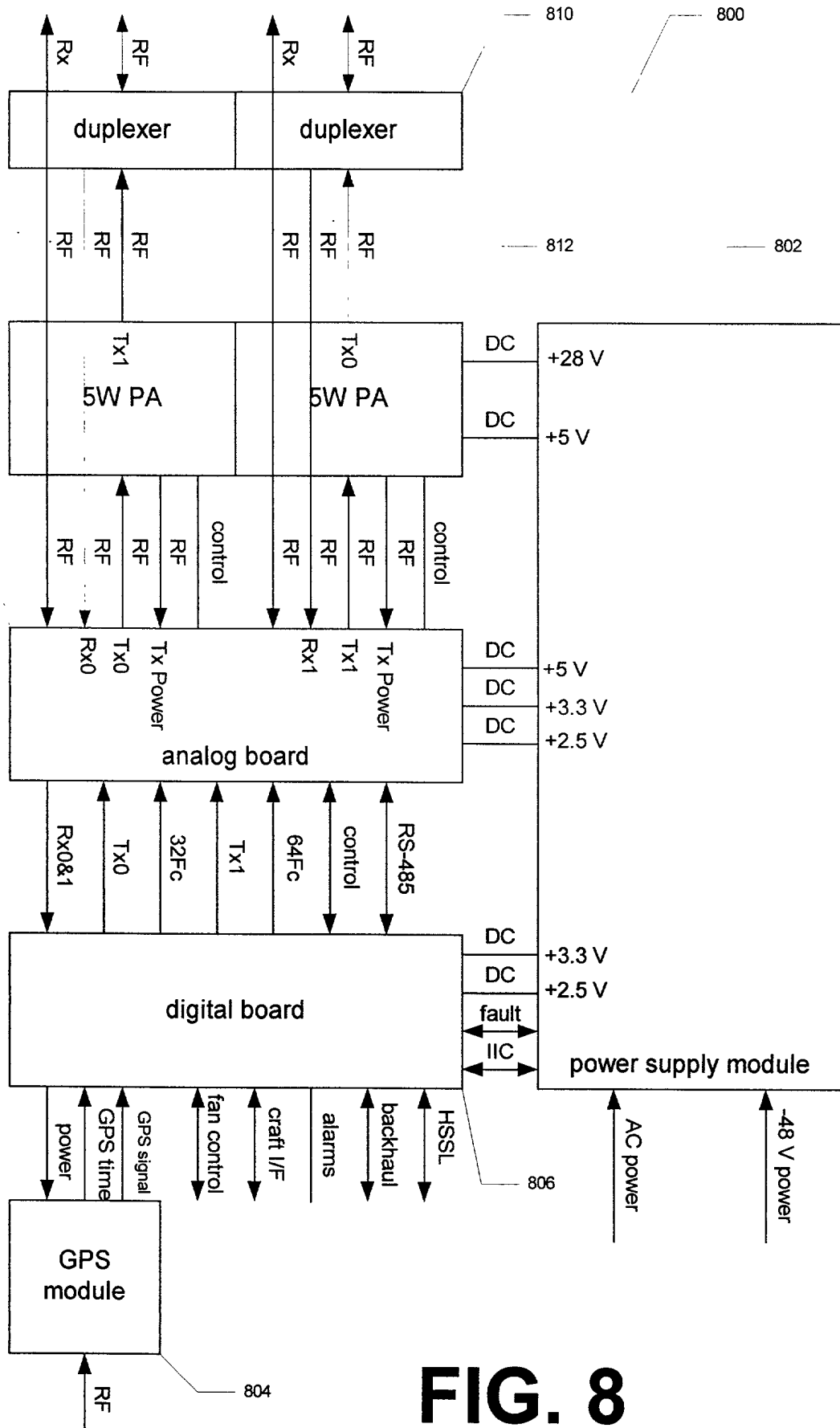


FIG. 8

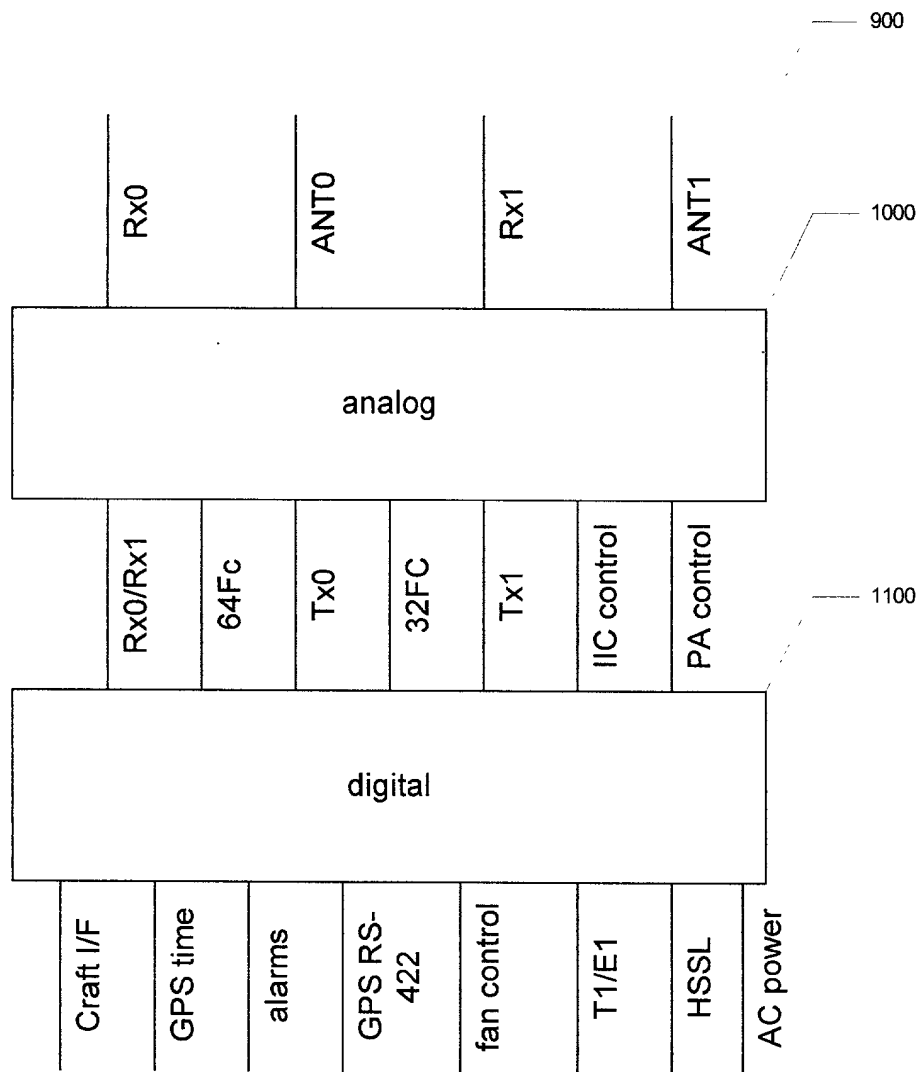


FIG. 9

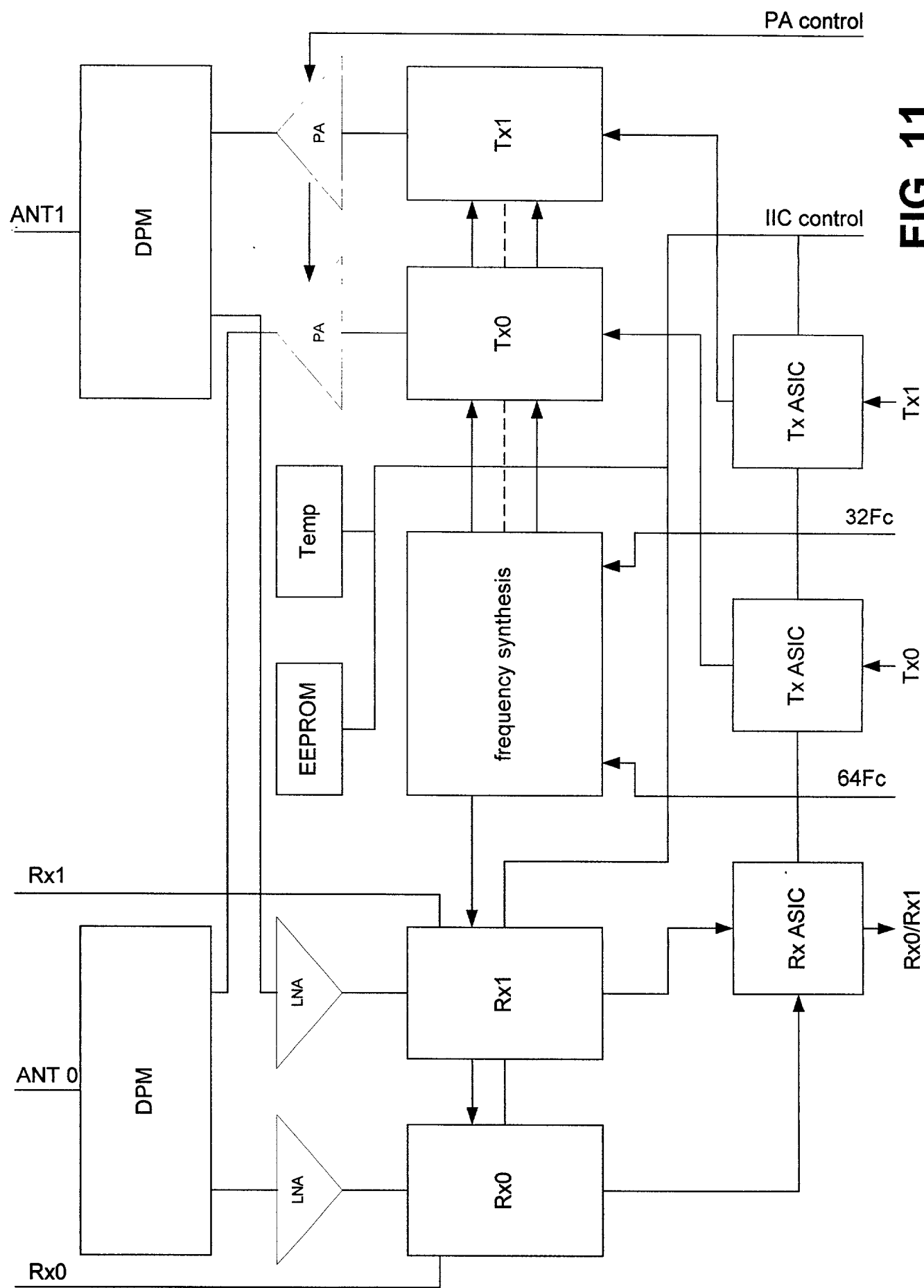


FIG. 11

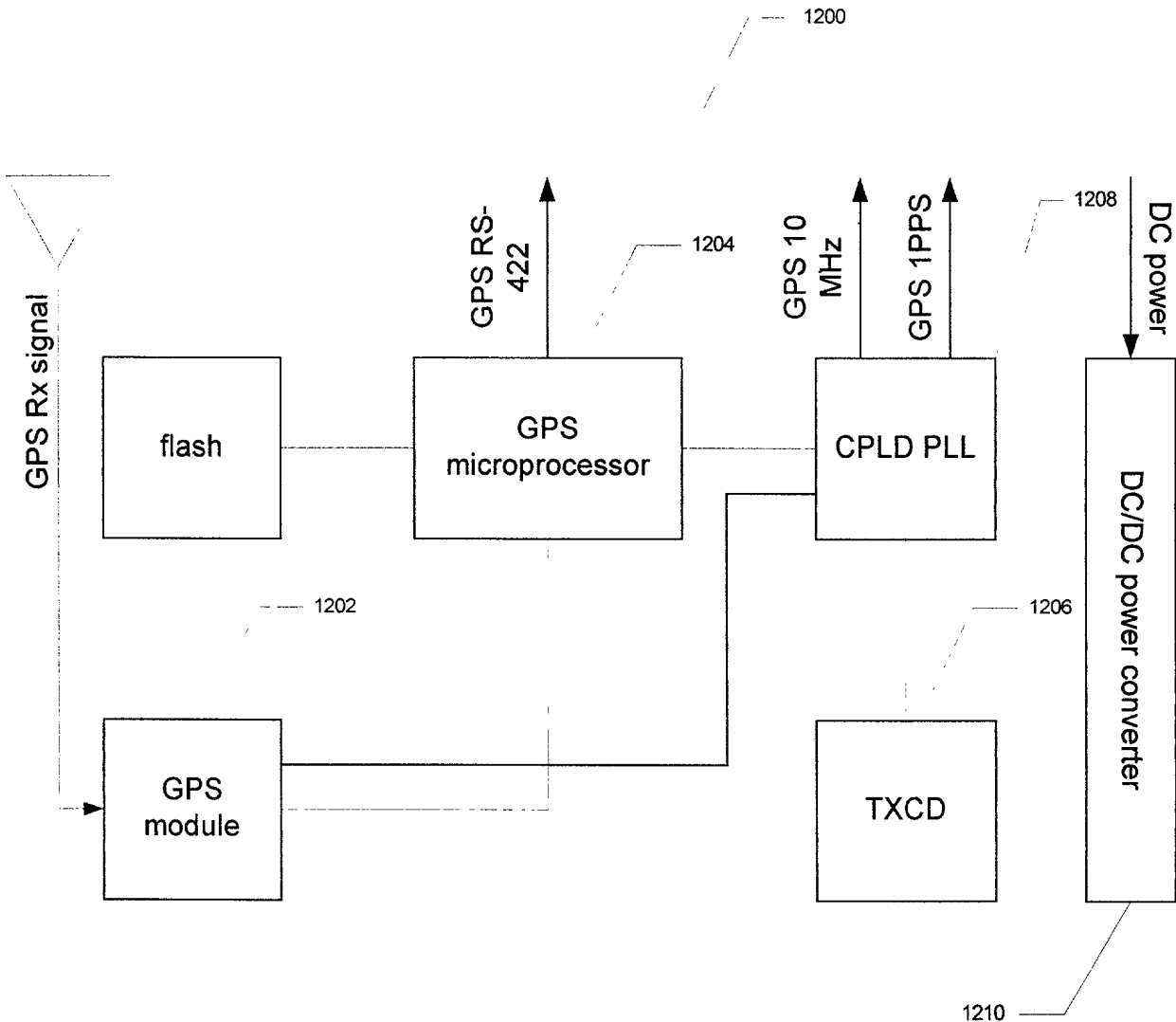


FIG. 12

FIG. 13 is a block diagram of a GPS receiver system 1300. The system includes a GPS Rx signal input, a GPS Rx block, a flash memory, a GPS microprocessor, a CPLD PLL, a DC/DC power converter, and a GPS module. The GPS Rx signal is received by the GPS Rx block, which is connected to the GPS module. The GPS module is connected to the GPS microprocessor, which is connected to the flash memory. The GPS microprocessor is also connected to the CPLD PLL, which provides a GPS 1PPS signal. The GPS microprocessor is connected to the DC/DC power converter, which provides DC power to the system.

1300

GPS Rx signal

GPS Rx block

flash

GPS microprocessor

CPLD PLL

DC/DC power converter

GPS module

GPS 1PPS

GPS RS-422

1302

1304

1306

FIG. 13

FIG. 14 is a block diagram of a power supply system 1400. The system includes an AC input, a breaker fuse EMI, an AC/DC power converter, a DC/DC converter, a filter, a PA module, a digital board CPLD, a charge controller, and an EMI filter. The AC input is connected to the breaker fuse EMI, which is connected to the AC/DC power converter. The AC/DC power converter outputs 48 V to the DC/DC converter and the EMI filter. The DC/DC converter outputs 28.0 V to the filter, which is connected to the PA module. The DC/DC converter also outputs 5.0 V to the analog board and 3.3 V to the analog and digital board. The charge controller is connected to the 48 V line and outputs 2.5 V to the analog and digital board. The digital board CPLD is connected to the 48 V line and provides control/on/off to the AC/DC power converter. The EMI filter is connected to the 48 V line and the EMI filter.

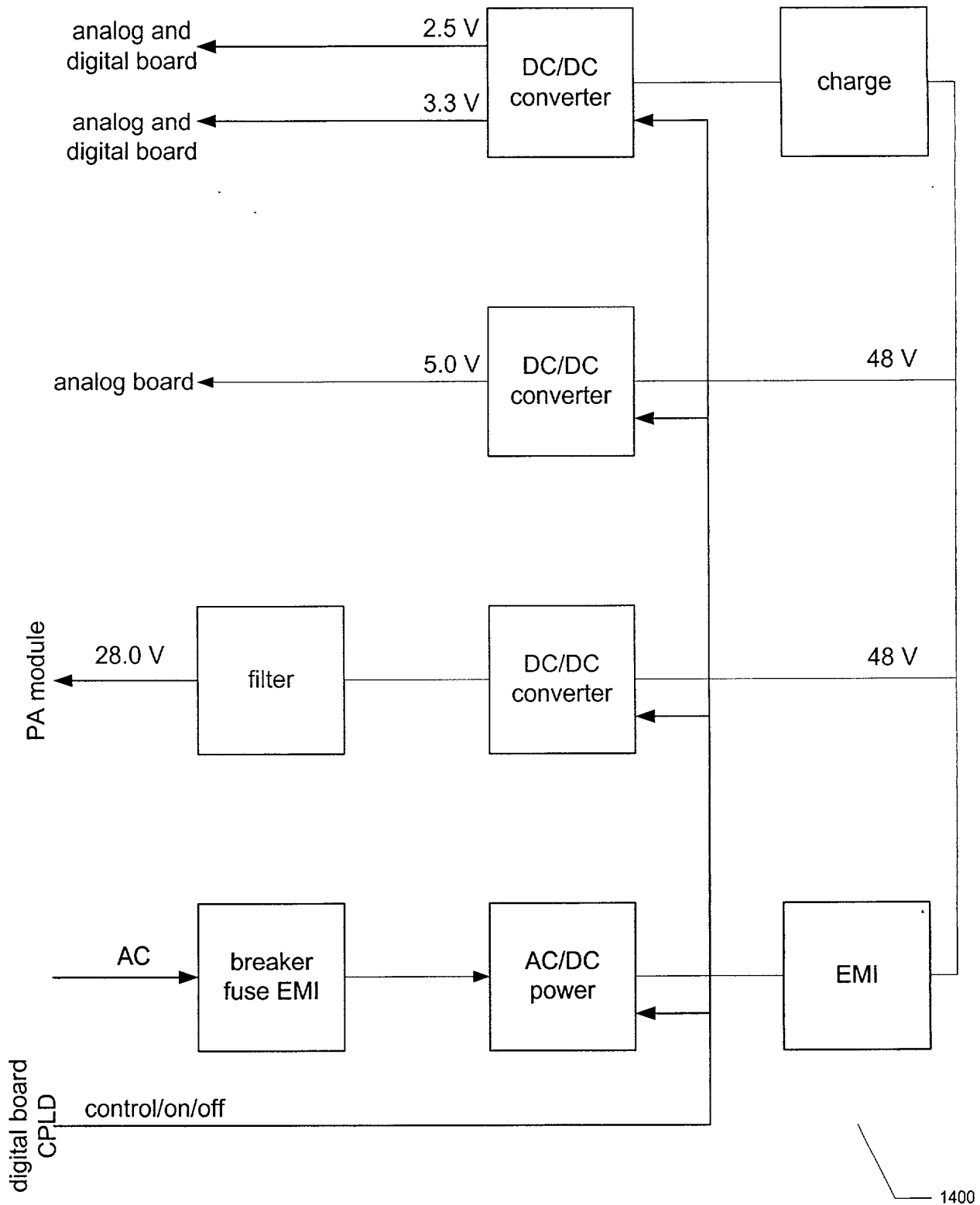


FIG. 14

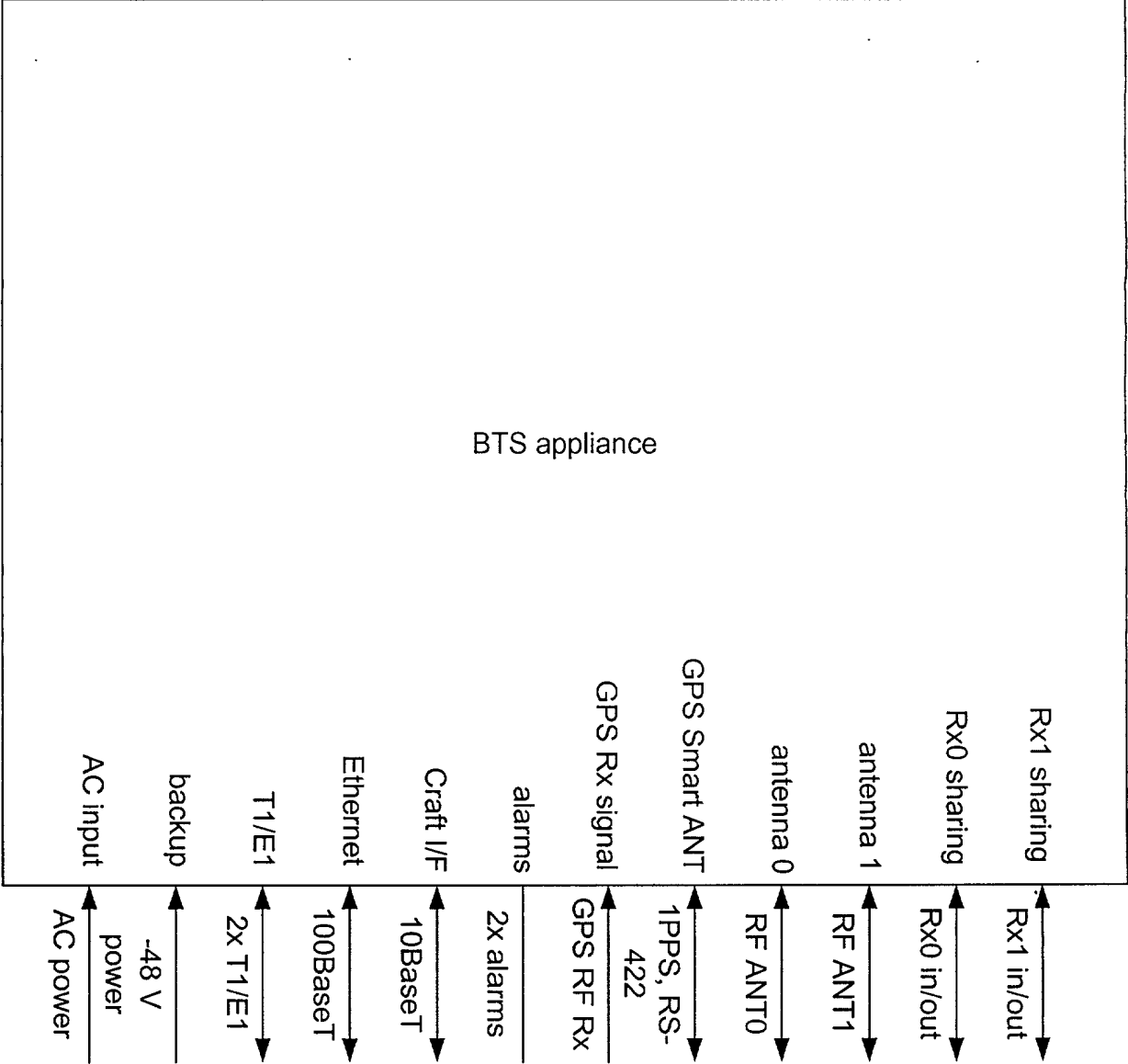


FIG. 15

FIG. 15 is a block diagram of a BTS appliance. The BTS appliance includes a Rx1 sharing interface, a Rx0 sharing interface, antenna 1, antenna 0, a GPS Smart ANT, a GPS Rx signal interface, an alarms interface, a Craft I/F interface, an Ethernet interface, a T1/E1 interface, a backup interface, an AC input interface, a Rx1 in/out interface, a Rx0 in/out interface, RF ANT1, RF ANT0, a 1PPS, RS-422 interface, a GPS RF Rx interface, a 2x alarms interface, a 10BaseT interface, a 100BaseT interface, a 2x T1/E1 interface, a -48 V power interface, and an AC power interface.

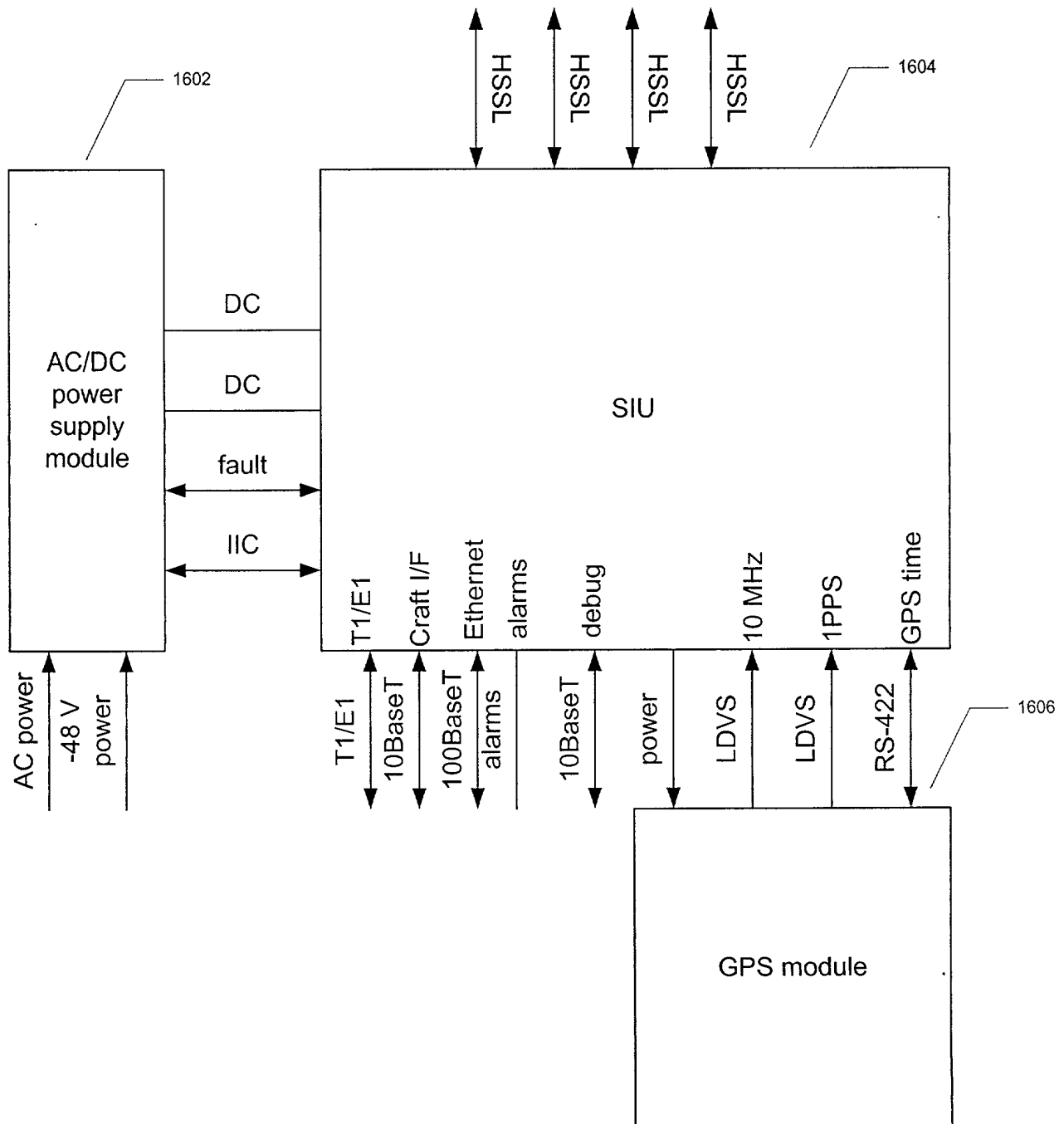


FIG. 16

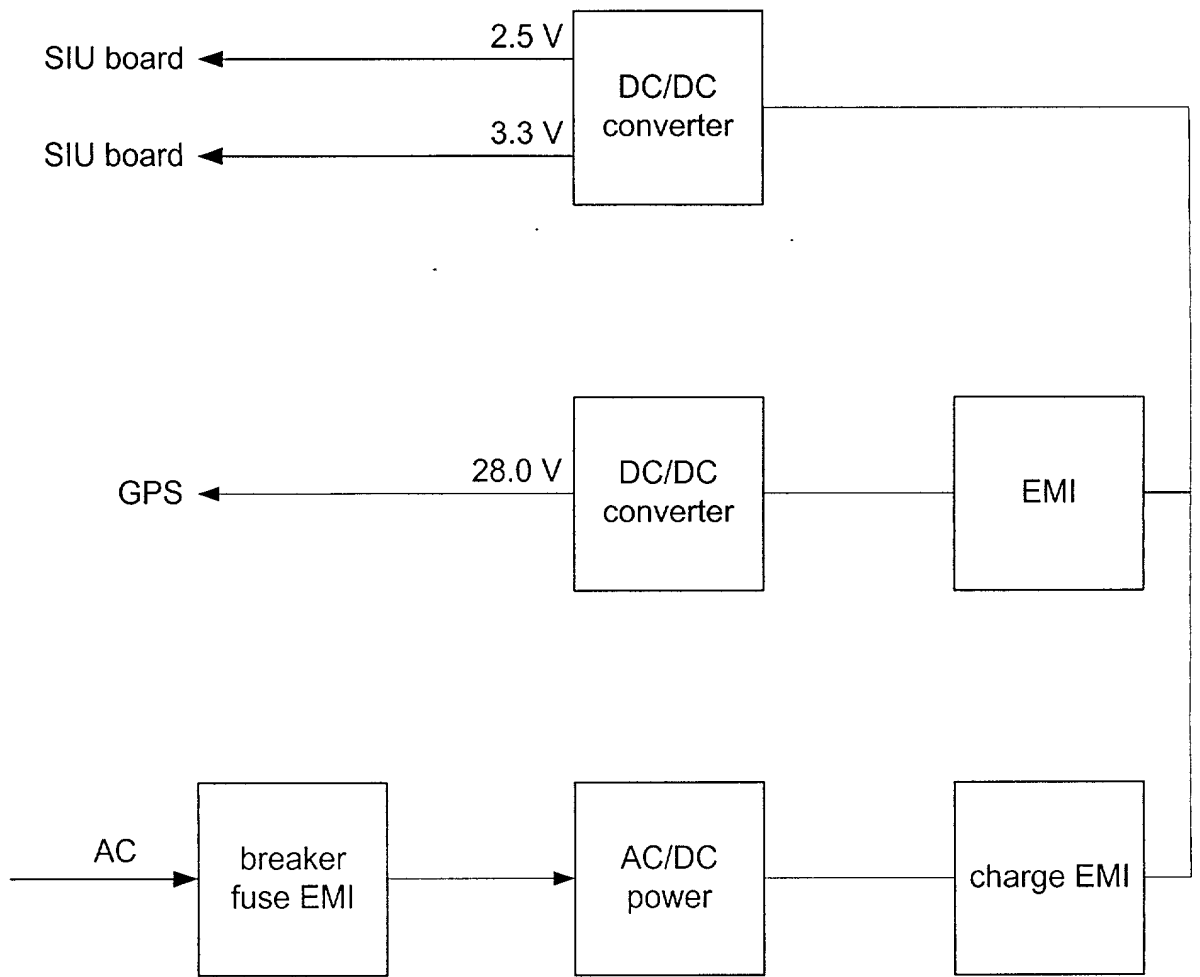


FIG. 18

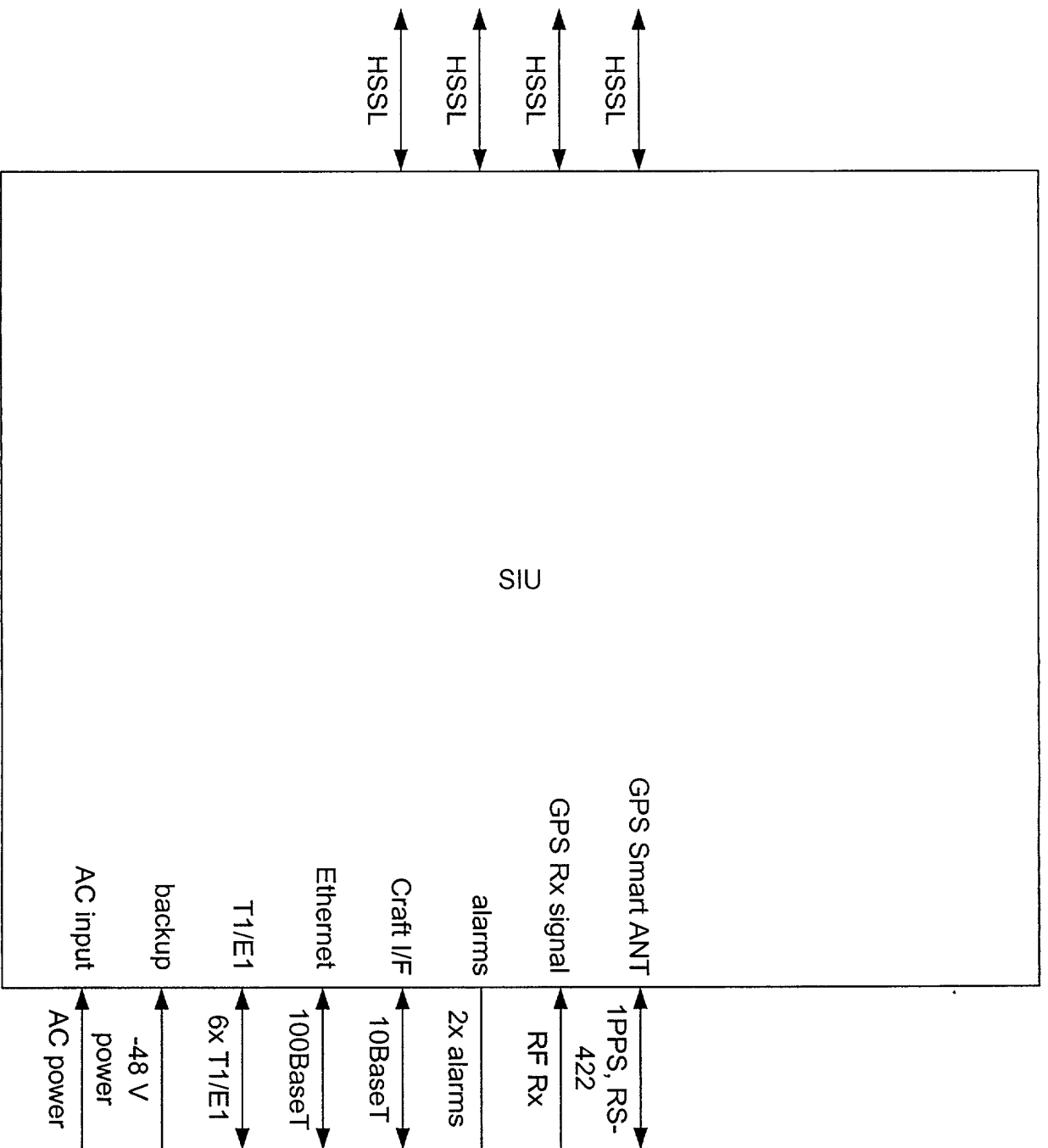


FIG. 19

FIG. 21 is a block diagram of a system architecture. The diagram is divided into three main sections: a top section for RF and Baseband (BB) processing, a middle section for digital baseband and control, and a bottom section for system integration and power management.

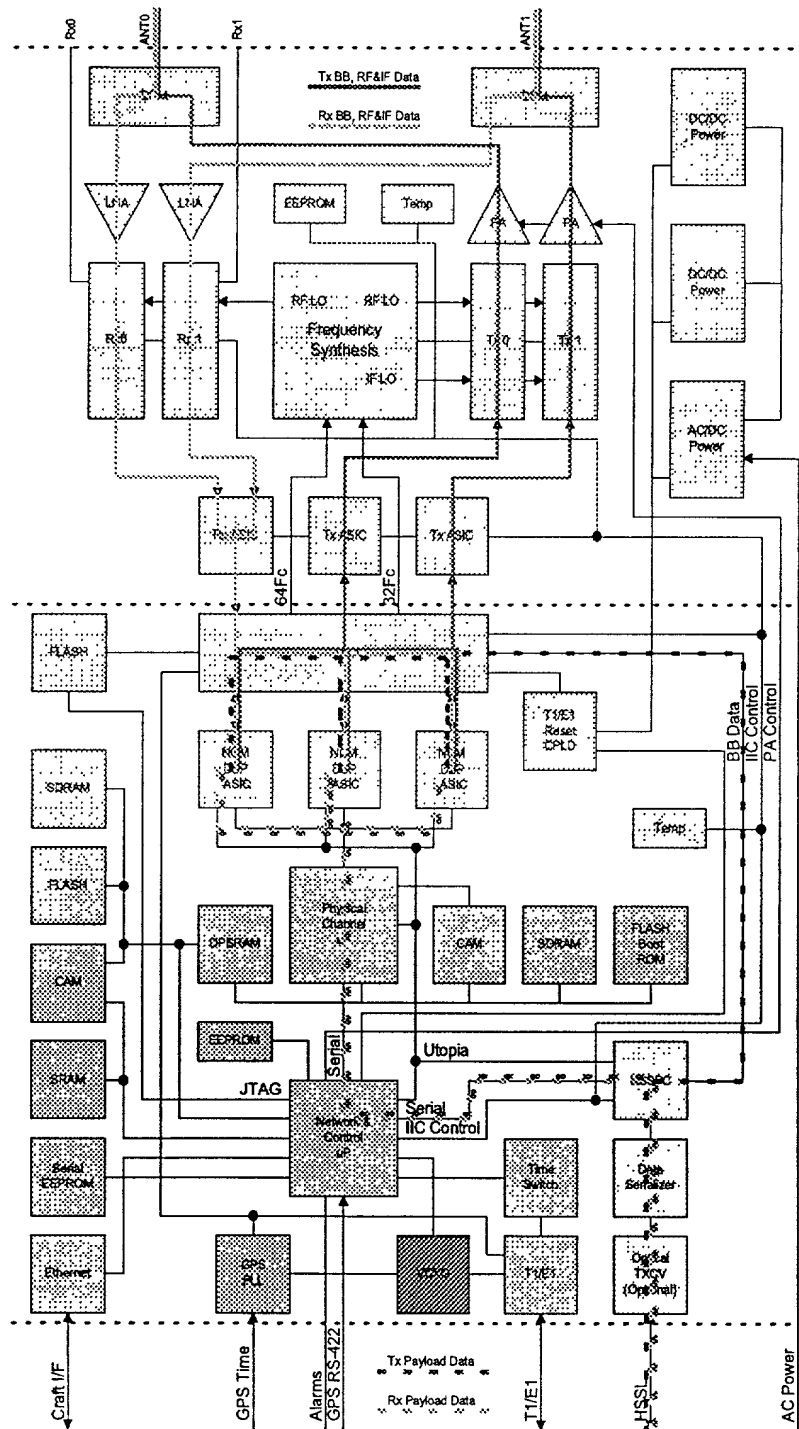


FIG. 21

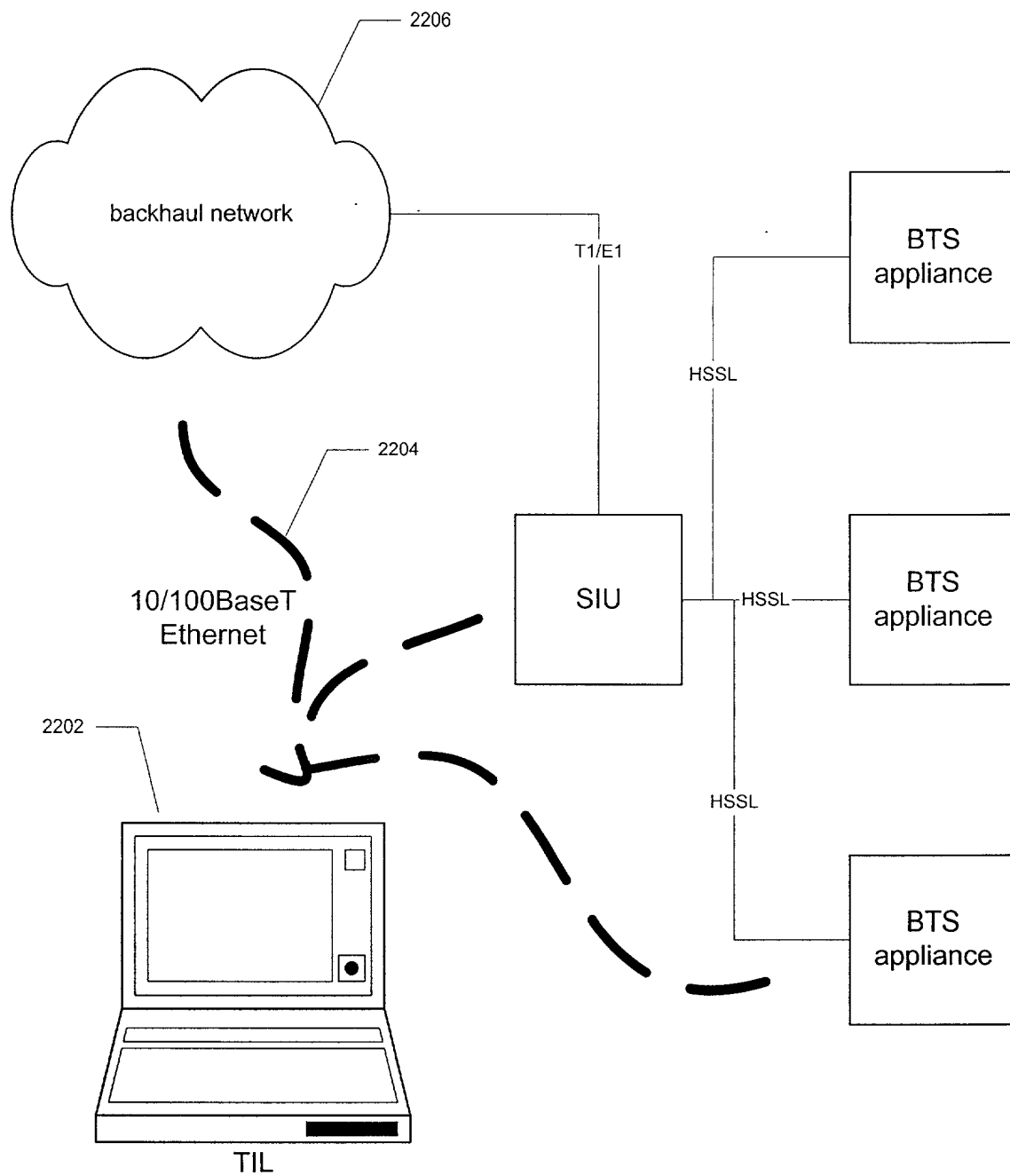


FIG. 22

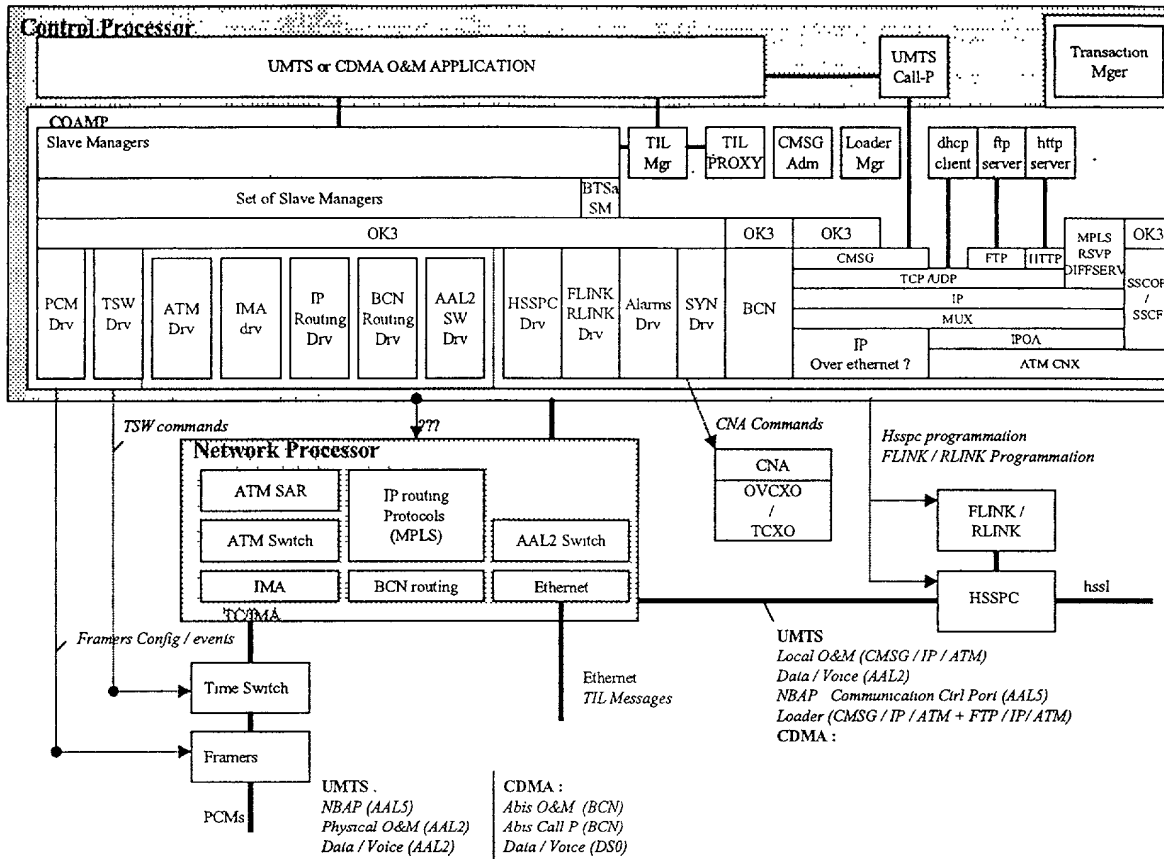


FIG. 23

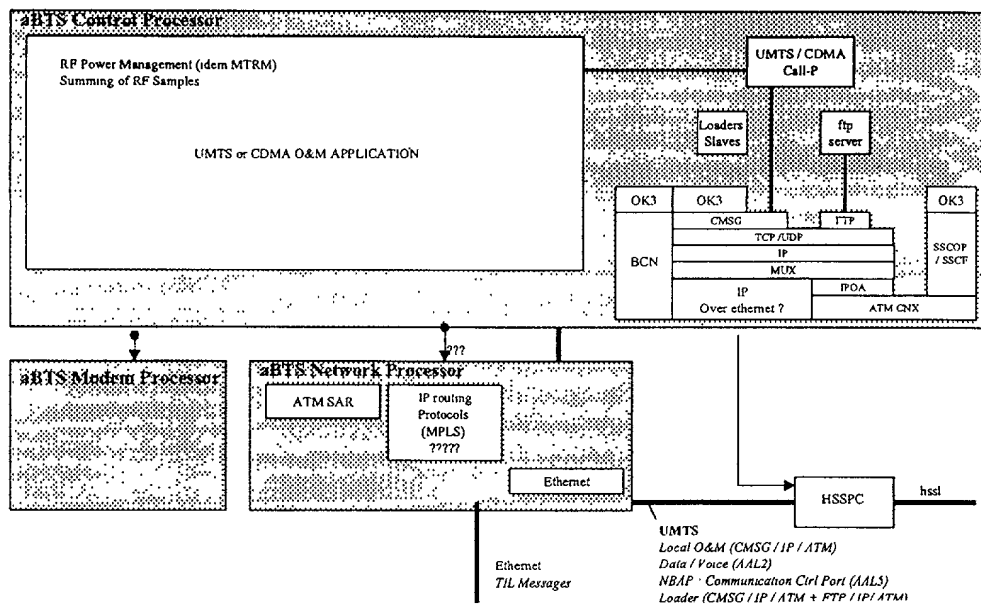


FIG. 24

2500

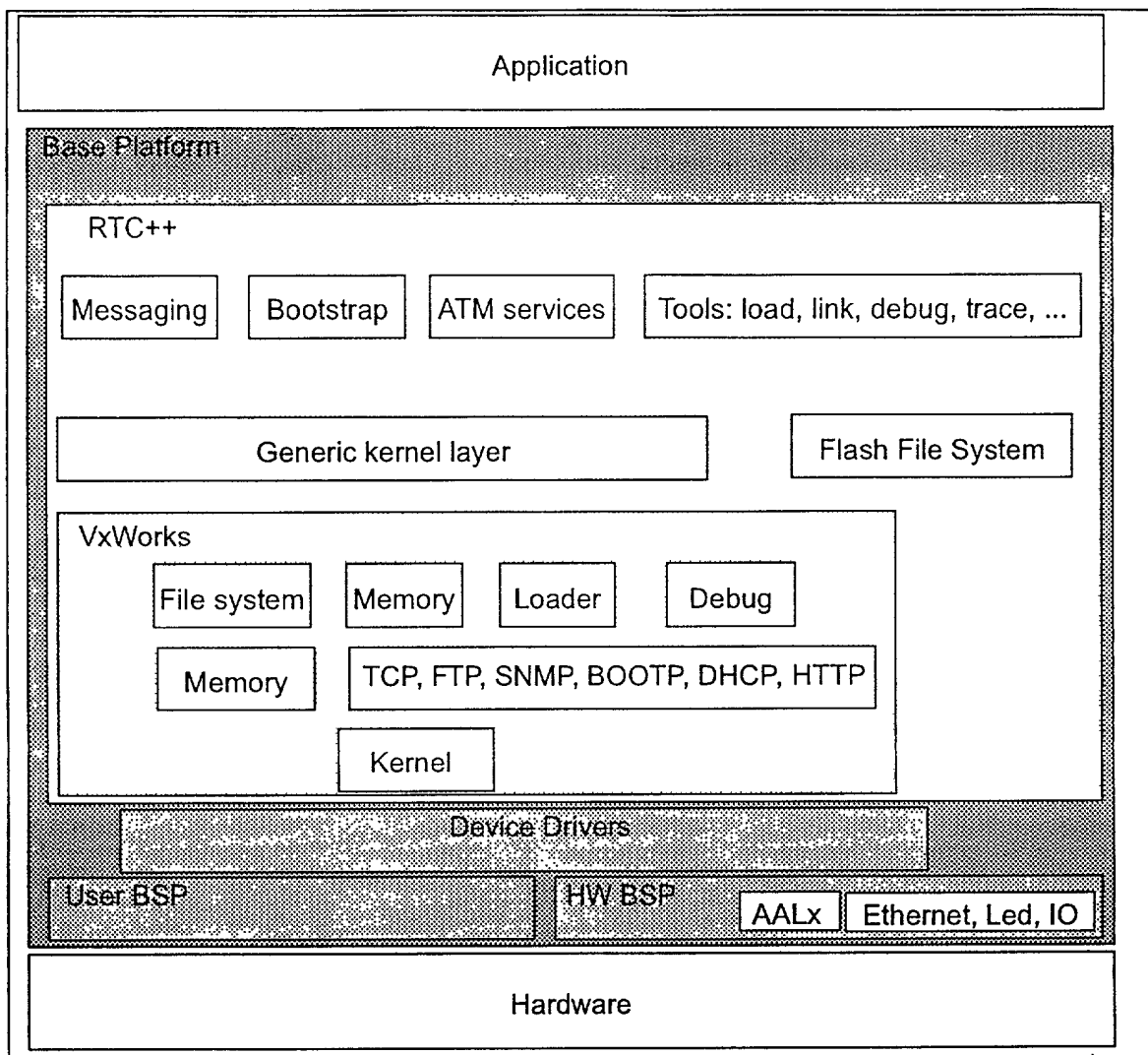


FIG. 25

2600

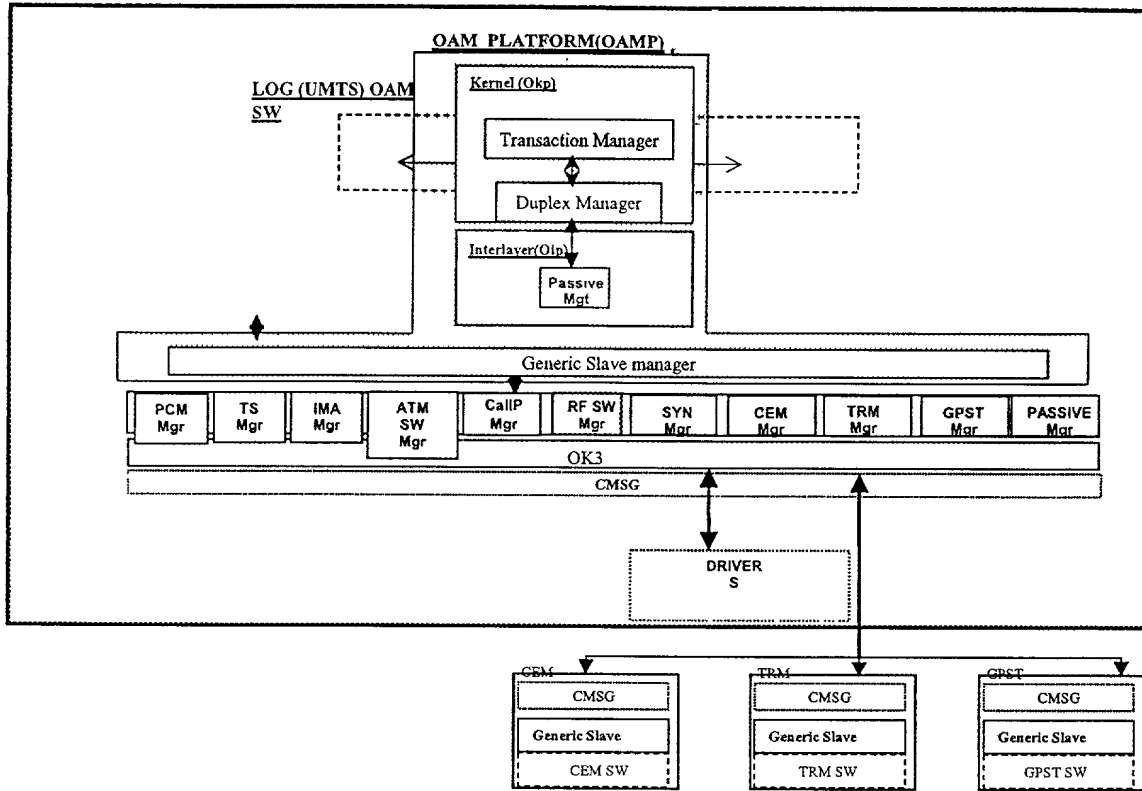


FIG. 26

12700

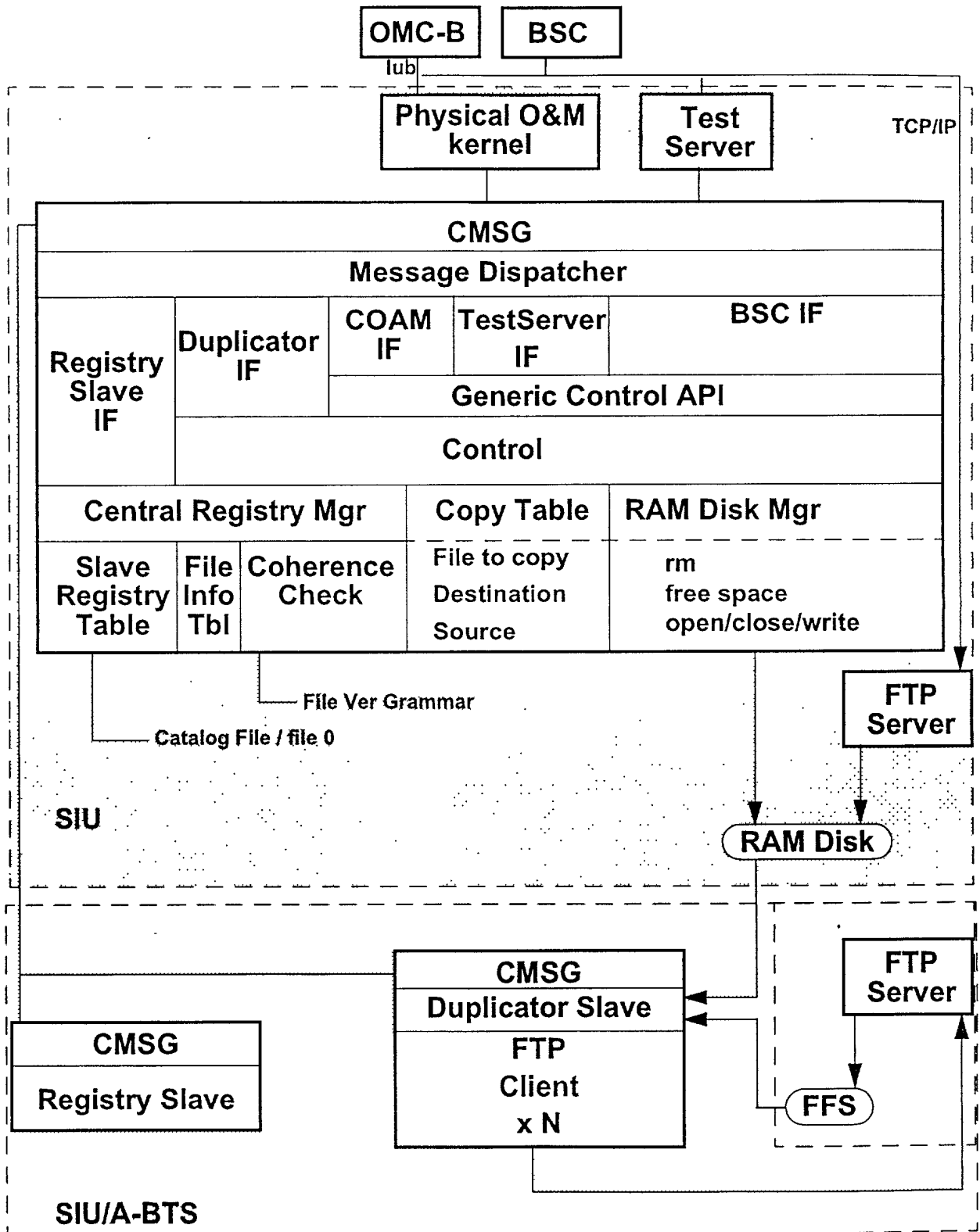


FIG. 27

2800

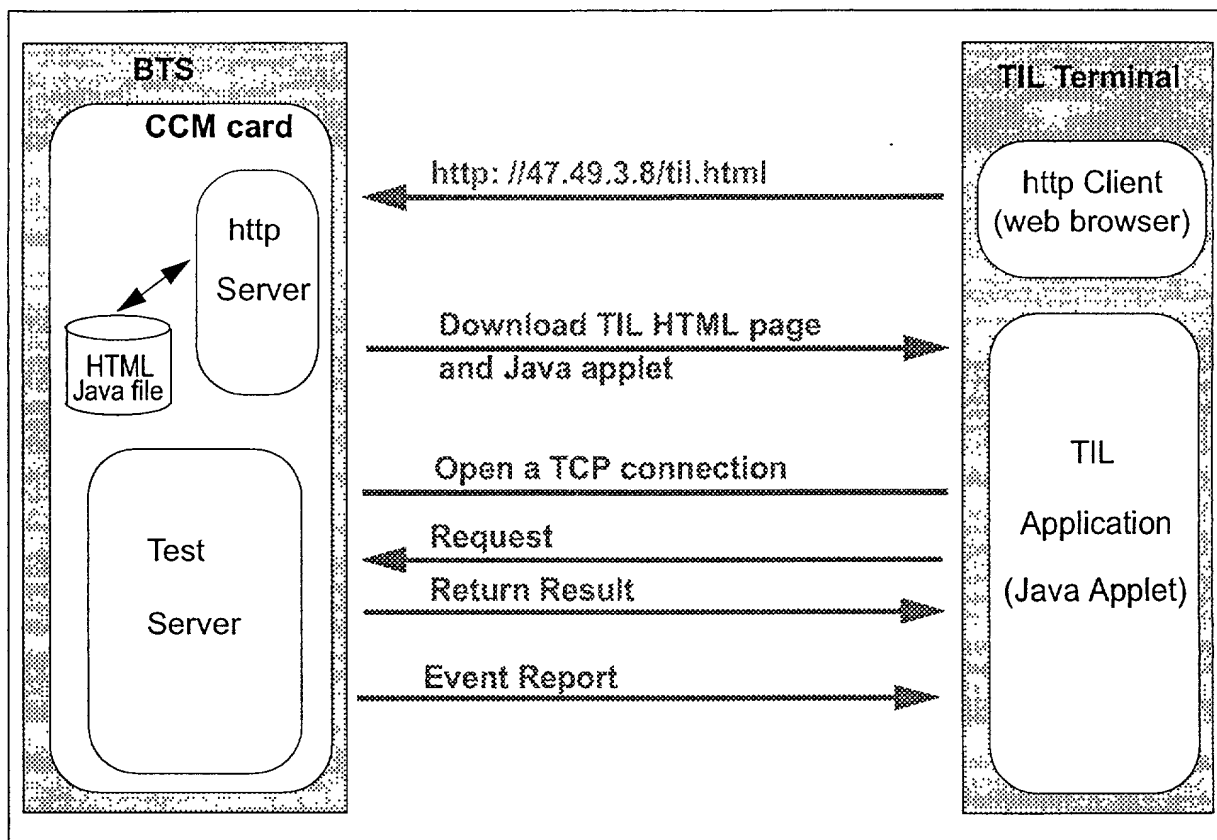
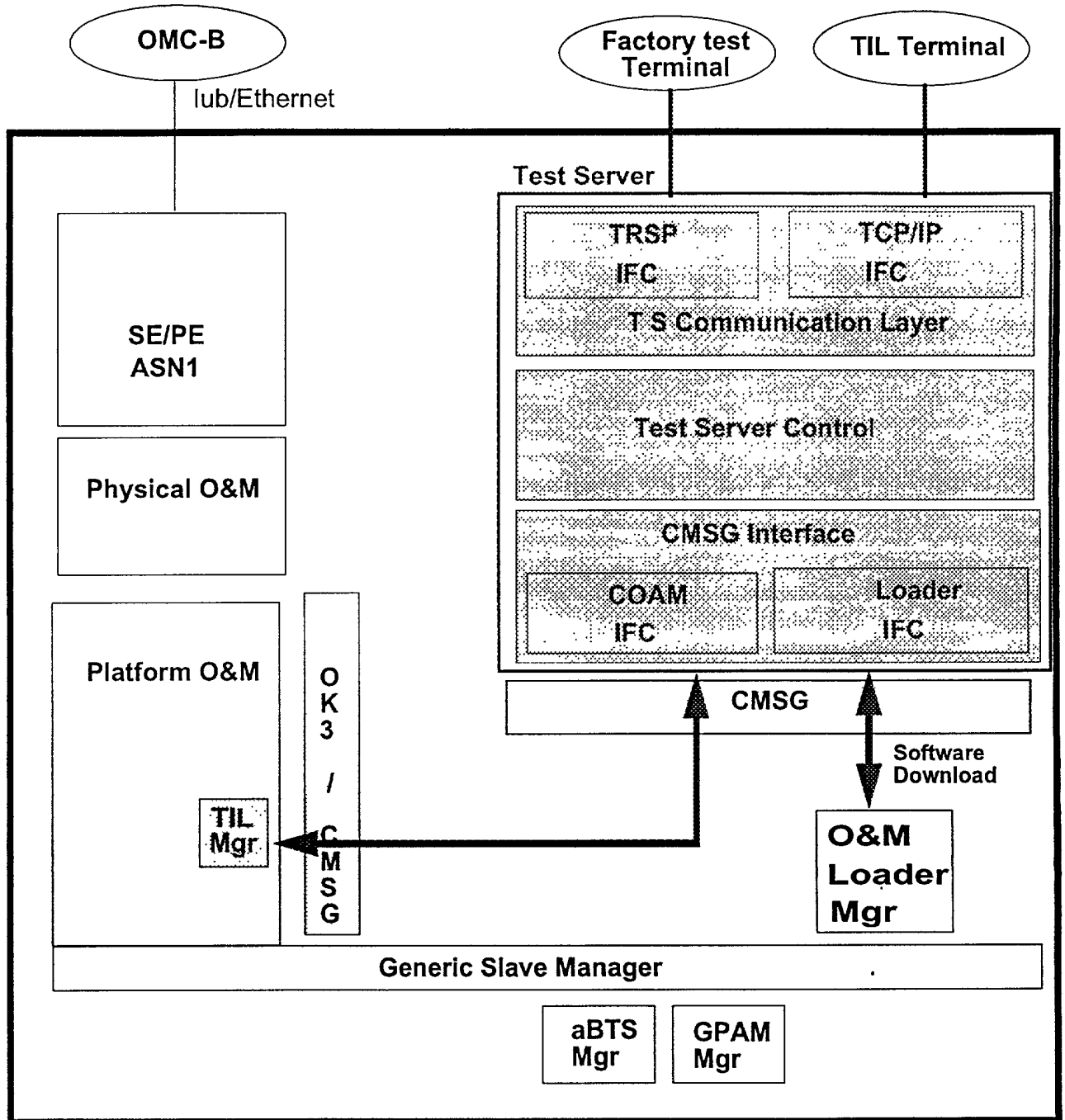


FIG. 28




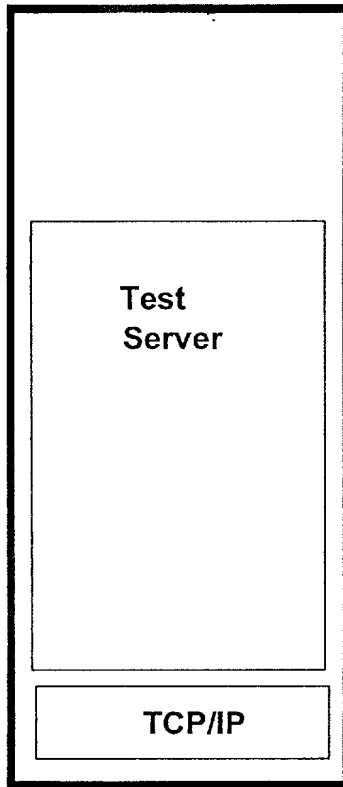
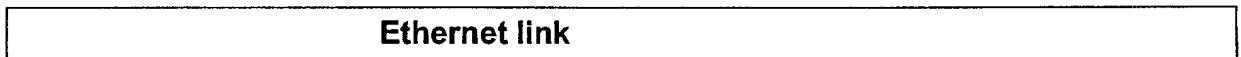
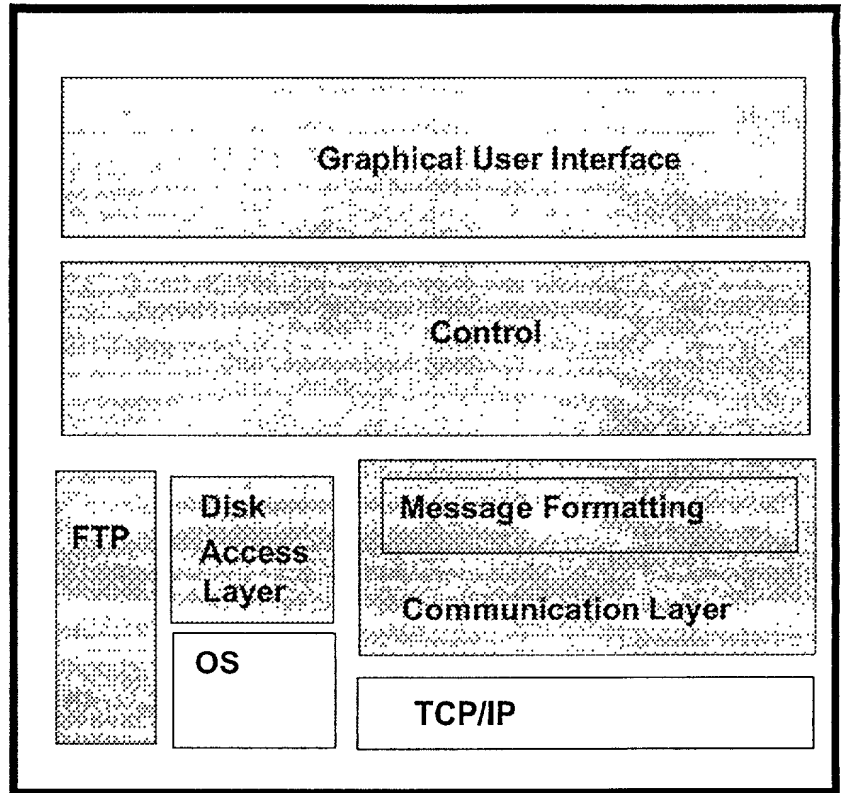
 Test Server layers

FIG. 29

SIU card



TIL Terminal



TIL Application Layers

FIG. 30

53100

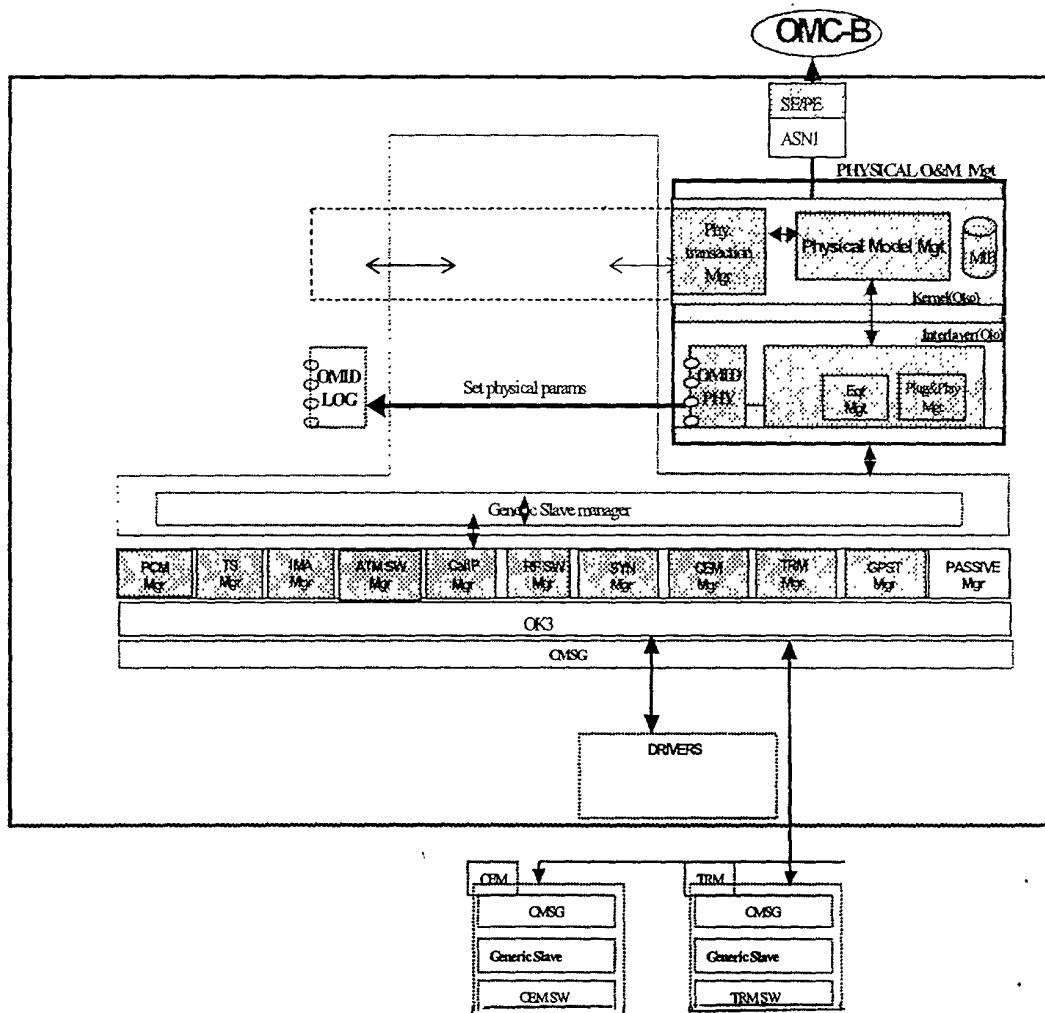
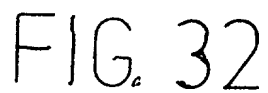


FIG. 31



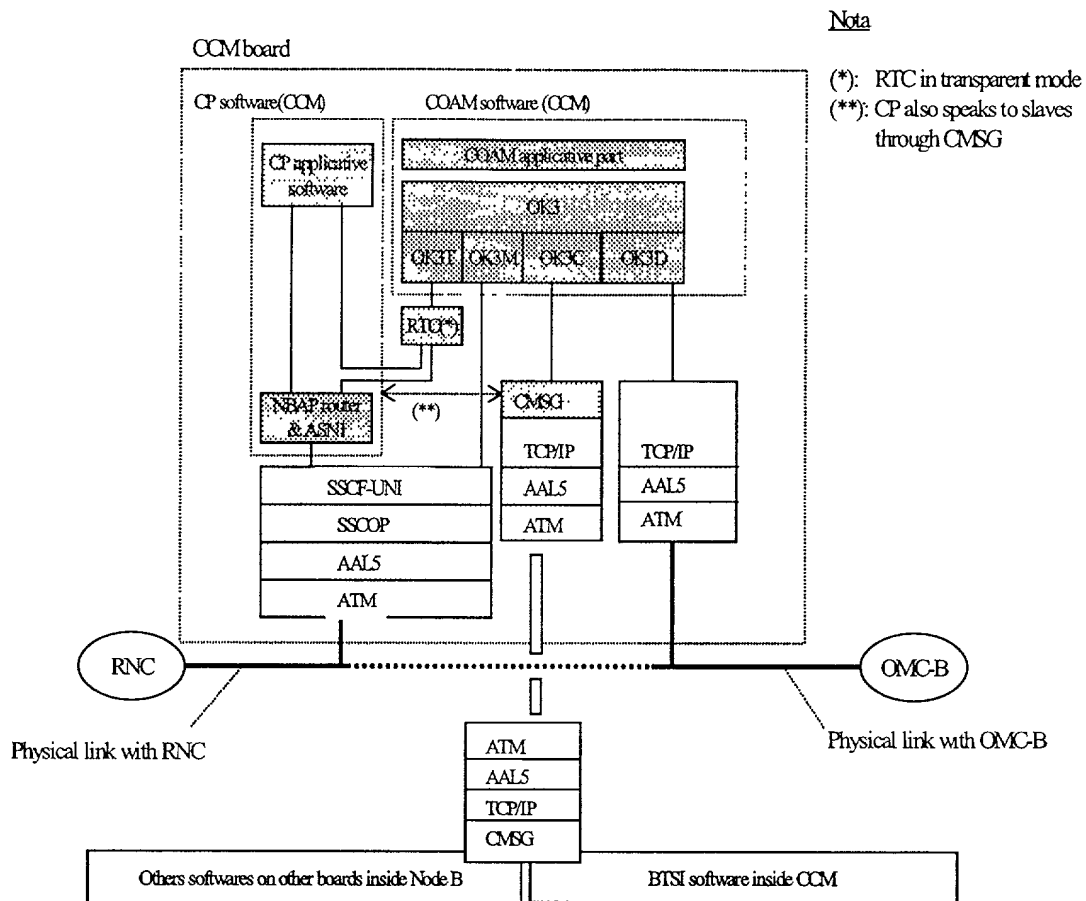


FIG. 33

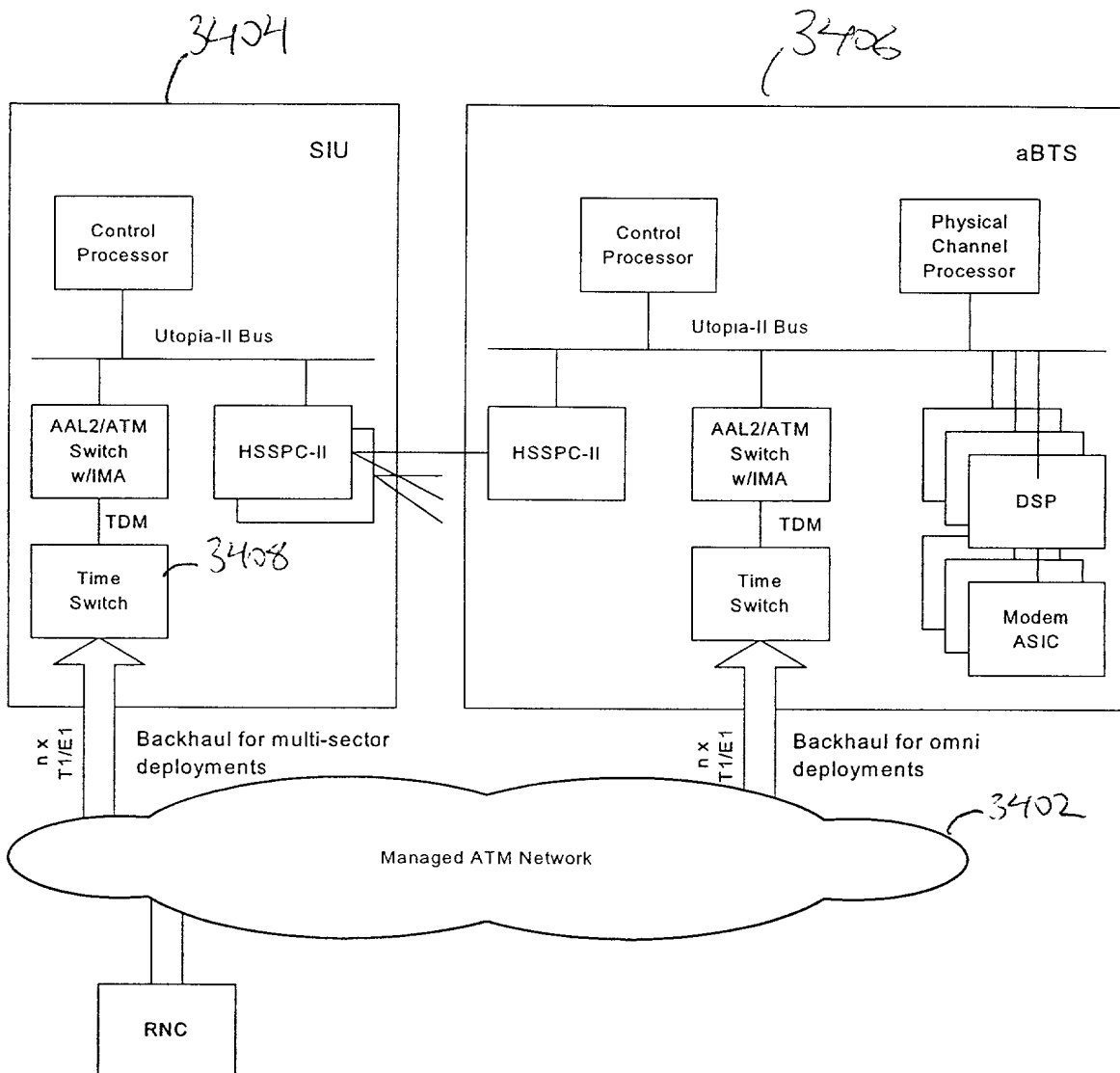


FIG. 34

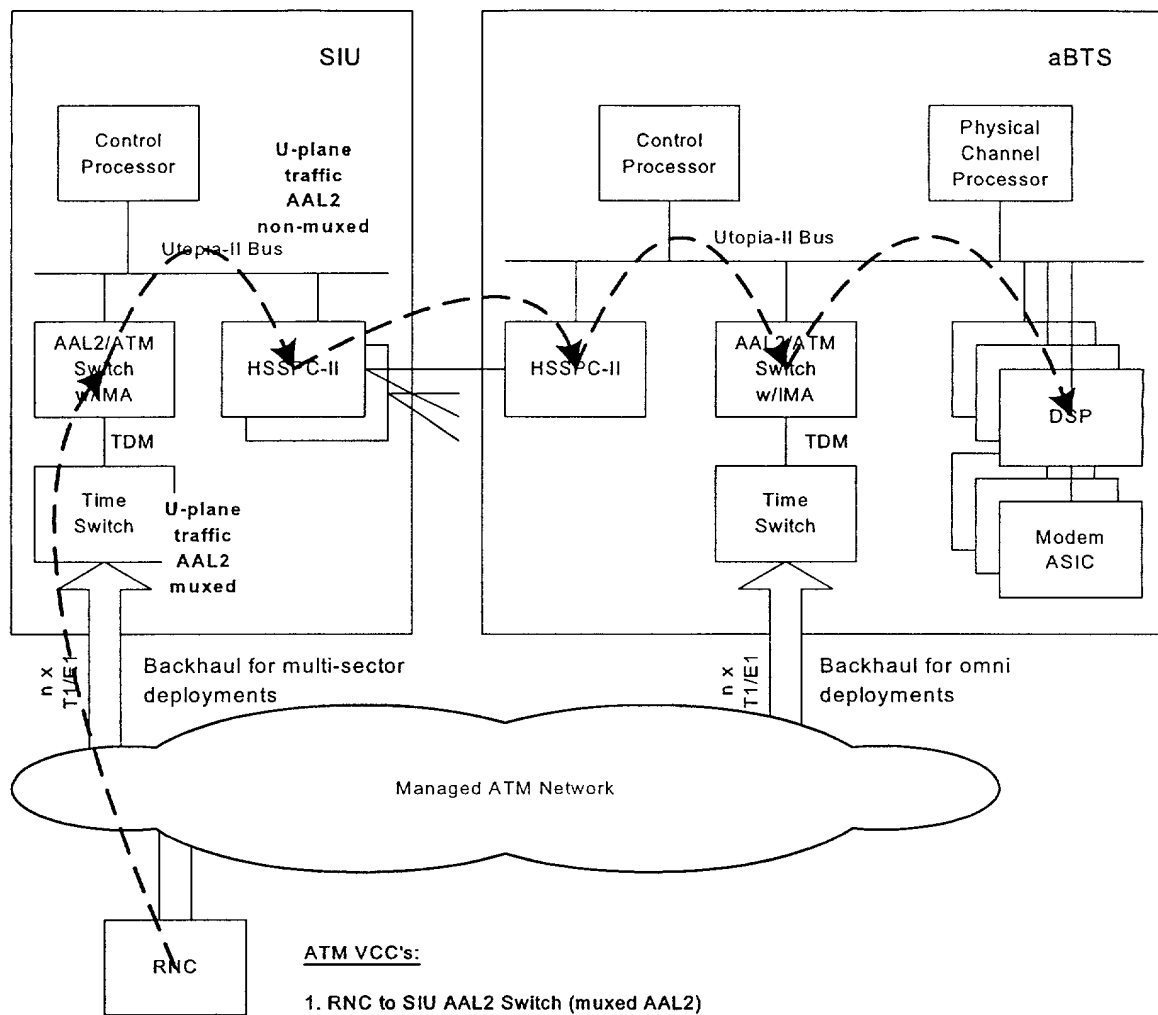


FIG. 35

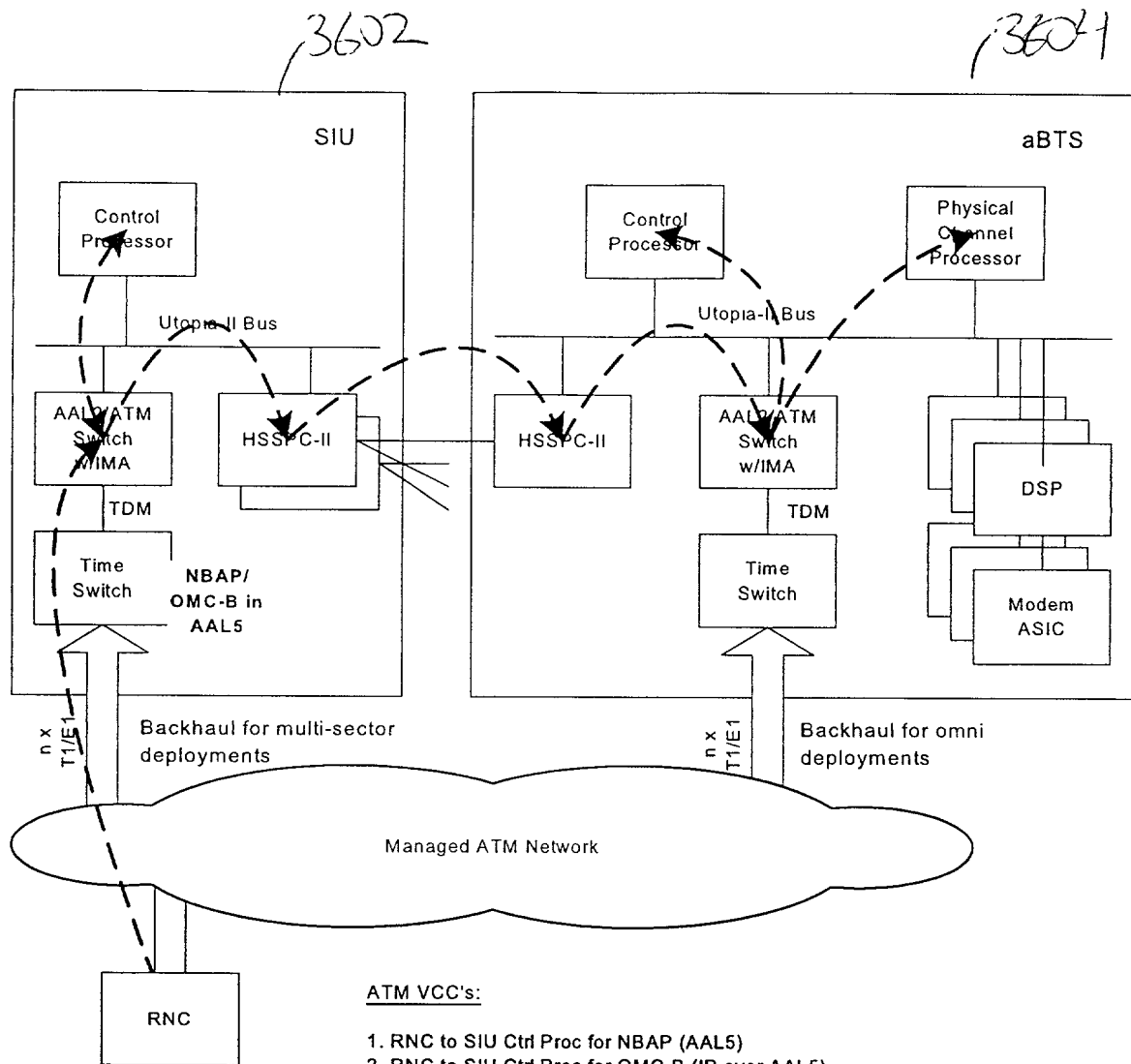
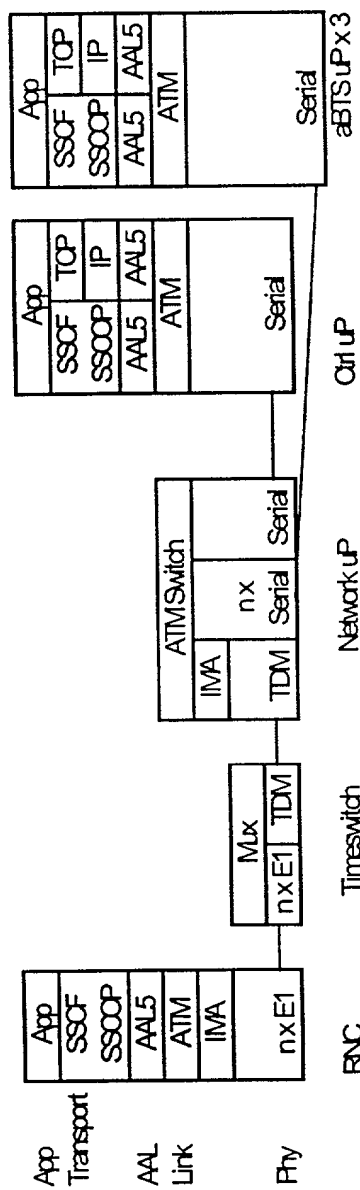


FIG. 36

UMTS'99 (ATM backhaul) NBAP Flow



FILE 637

FIG. 38 is a block diagram of a multi-homed network architecture for a UMTS '99 (ATM backhaul) OM-C-B Flow. The diagram illustrates the flow of data from a mobile station (MS) through a radio network controller (RNC) and a core network to a service provider network (SPN). The MS is shown with a protocol stack including Application (App), Transport (TCP), Network (IP), and Link (ATM, AAL5) layers. The RNC is shown with a protocol stack including Application (App), Transport (TCP), Network (IP), and Link (ATM, AAL5) layers. The core network is shown with a protocol stack including Application (App), Transport (TCP), Network (IP), and Link (ATM, AAL5) layers. The SPN is shown with a protocol stack including Application (App), Transport (TCP), Network (IP), and Link (ATM, AAL5) layers. The diagram also shows the physical layer (Phy) and the network layer (Network) components. The flow of data is indicated by arrows, showing the path from the MS through the RNC and the core network to the SPN.

UMTS '99 (ATM backhaul) OM-C-B Flow

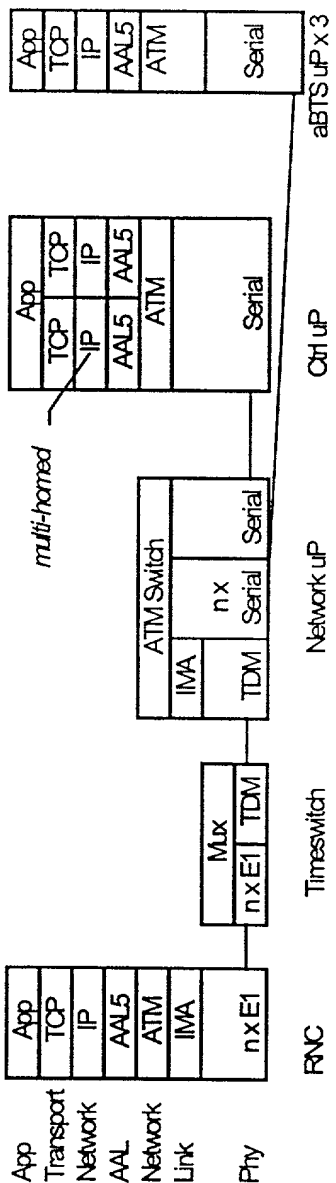


FIG. 38

UMTS '99 (ATM backhaul) User Flow

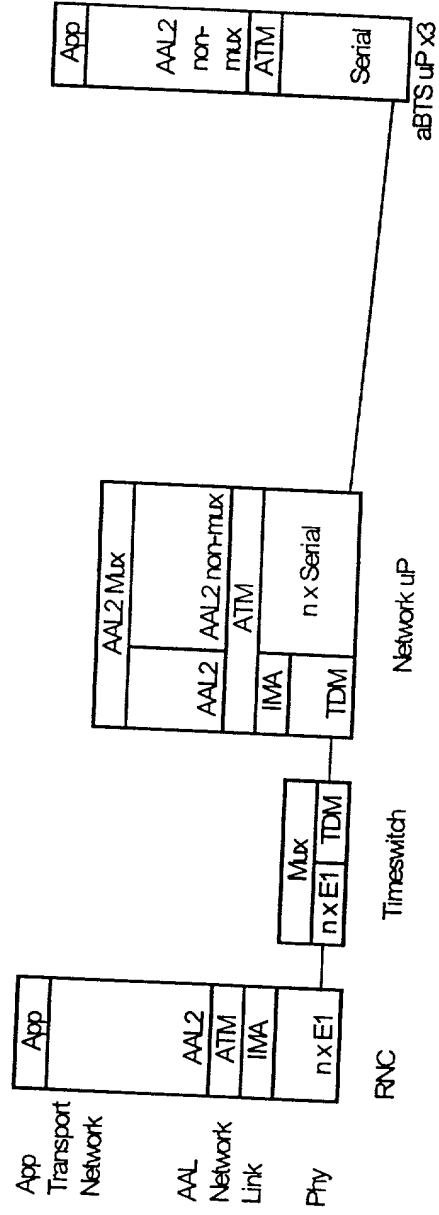
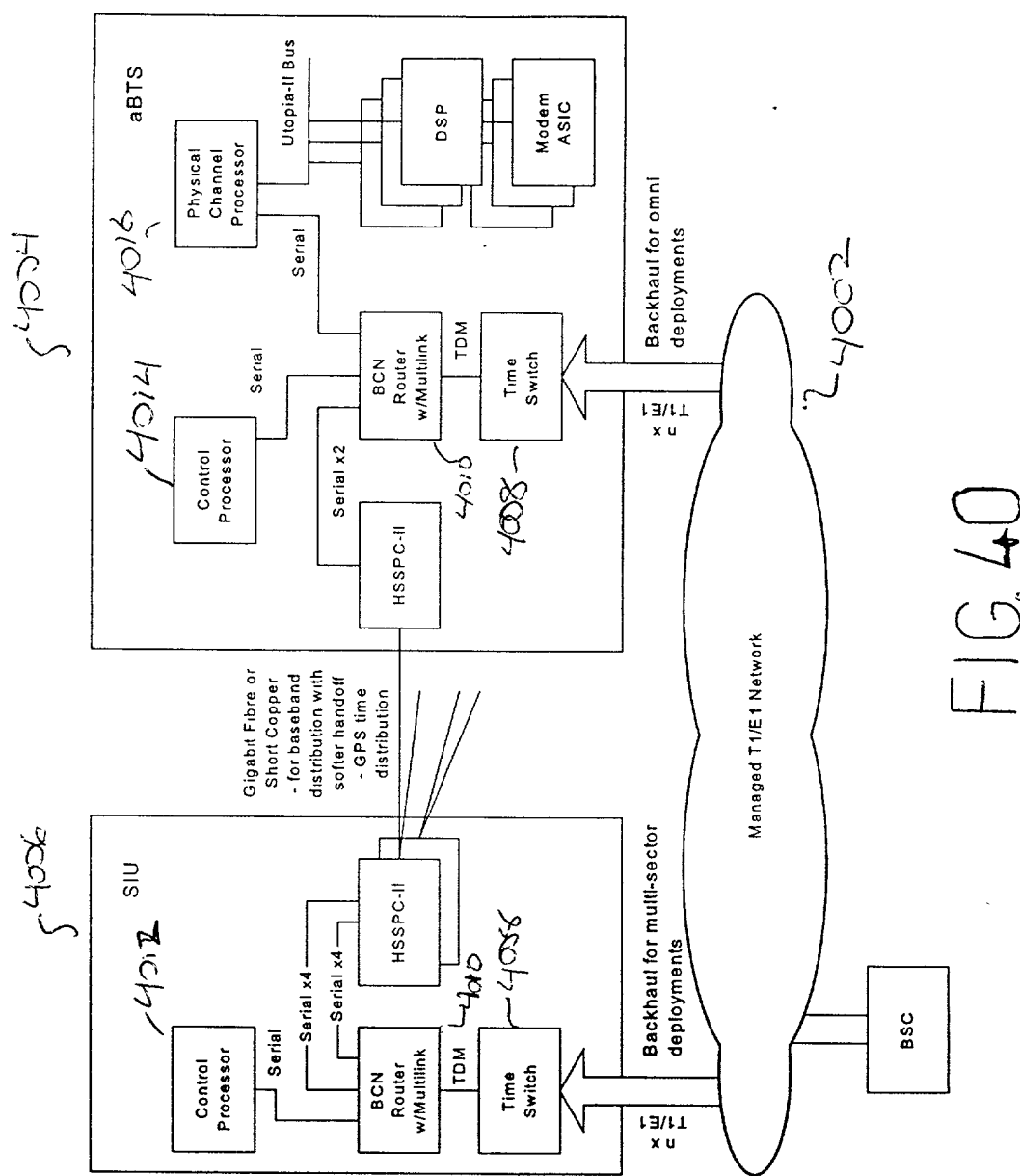
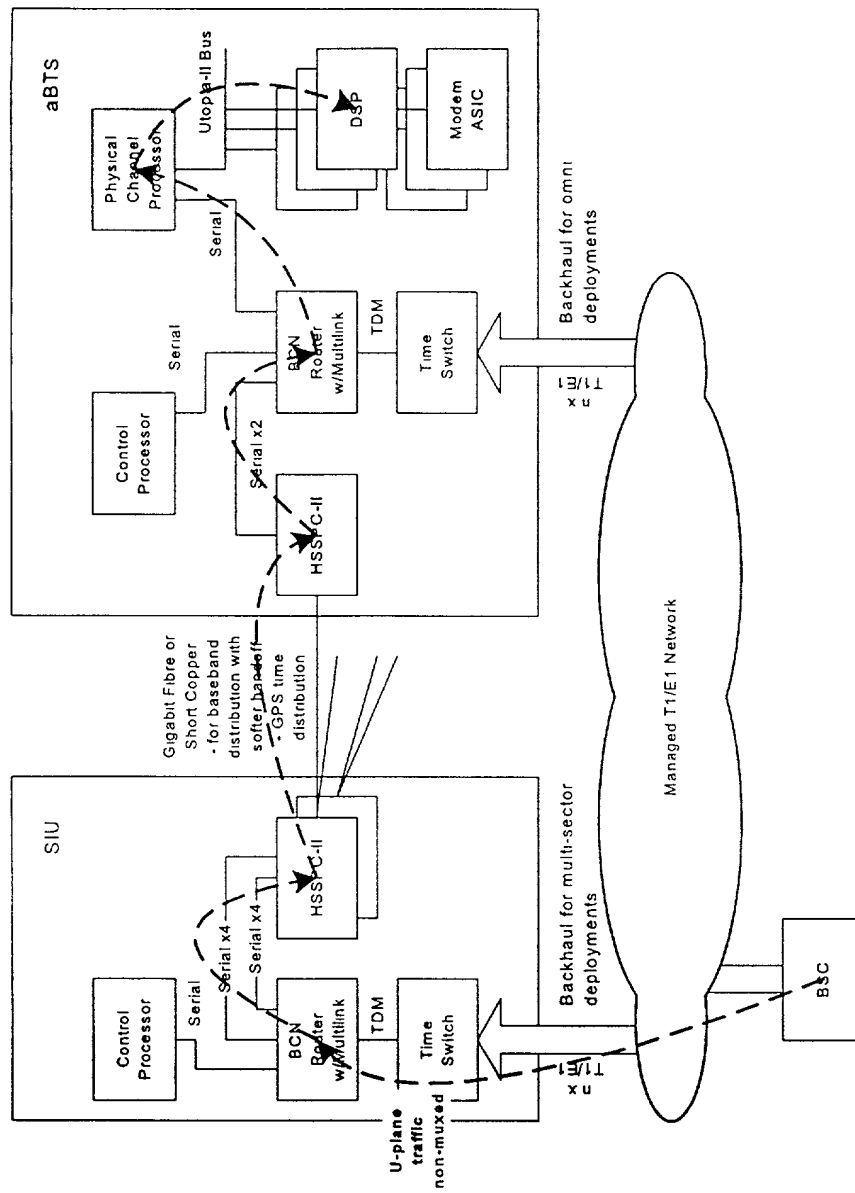


FIG. 39



07G1F



FILE 17

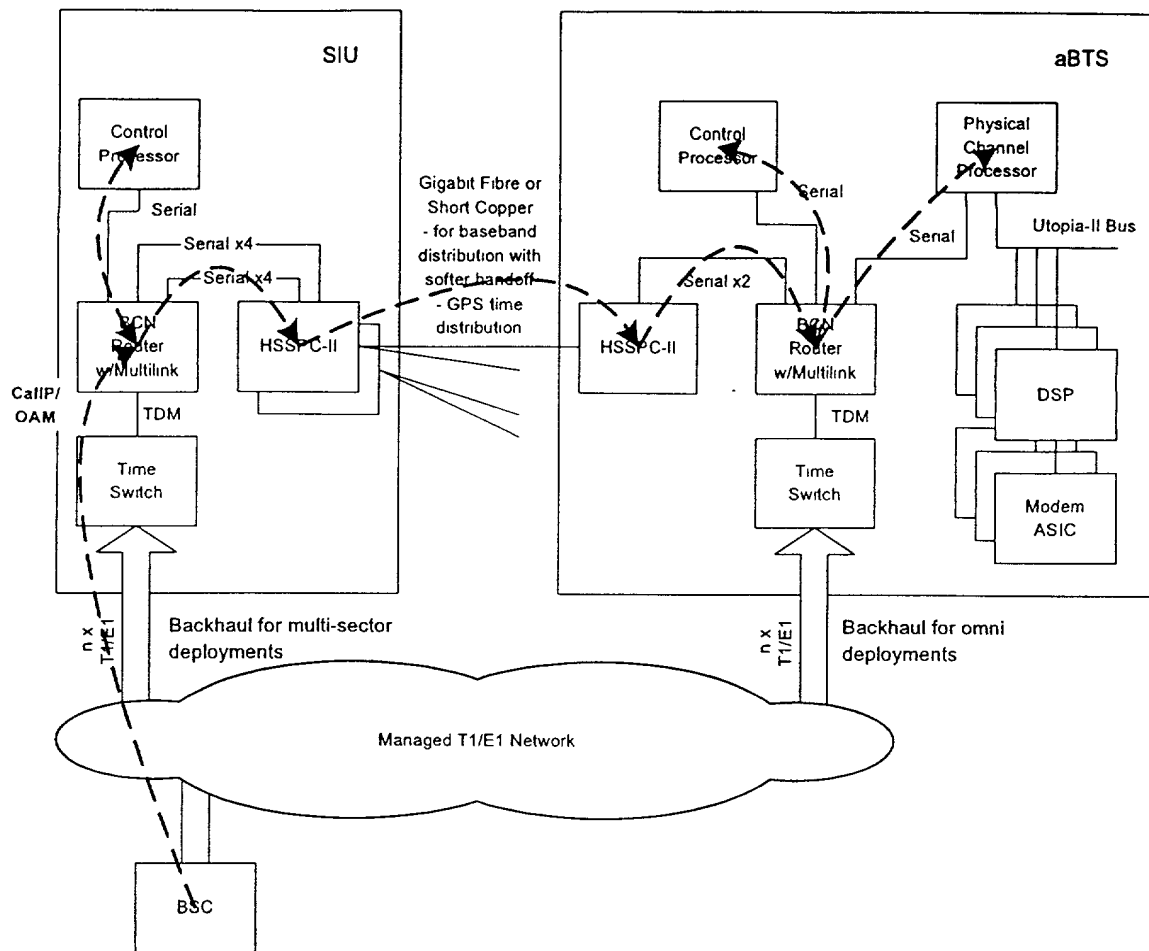


FIG. 42

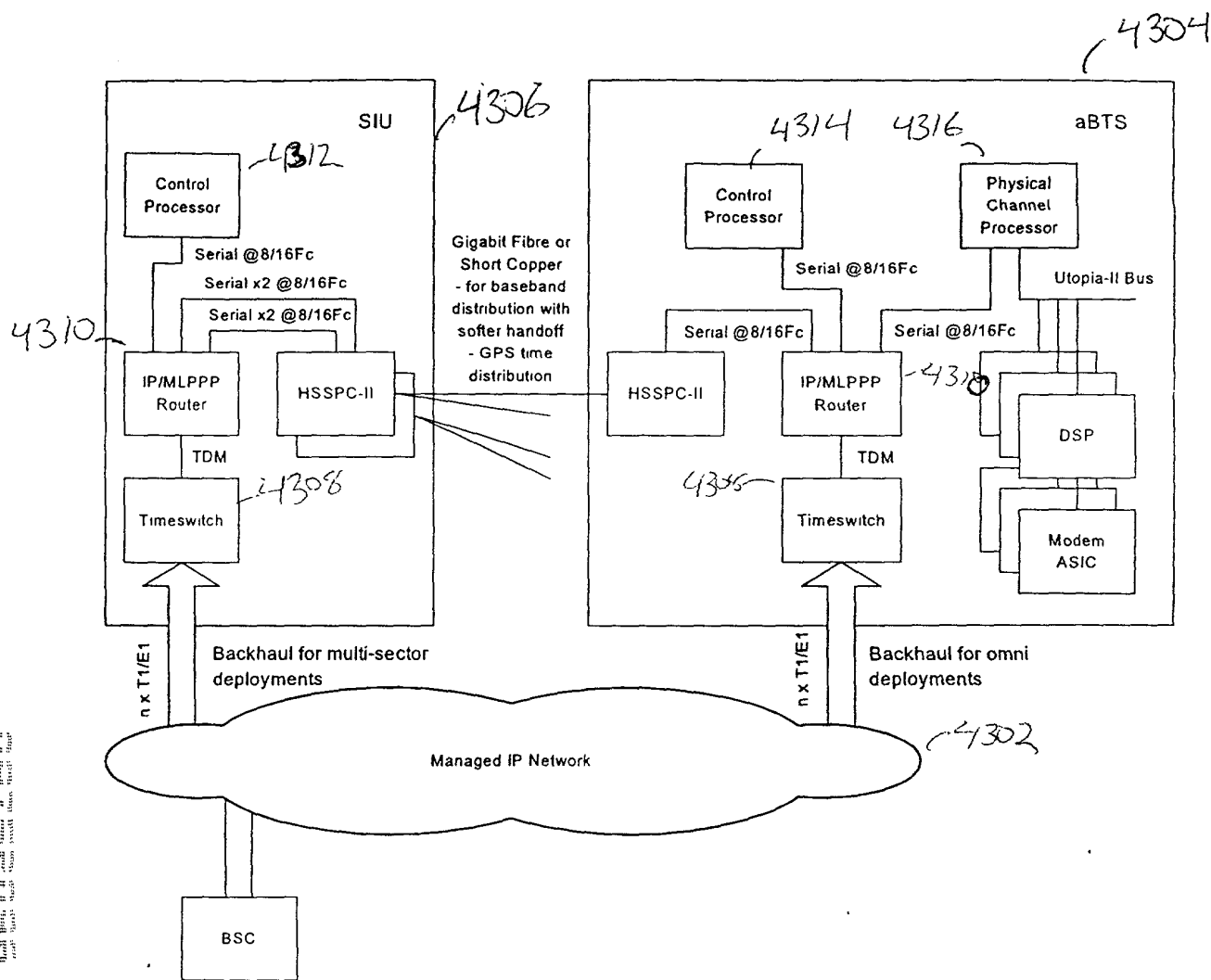


FIG. 43

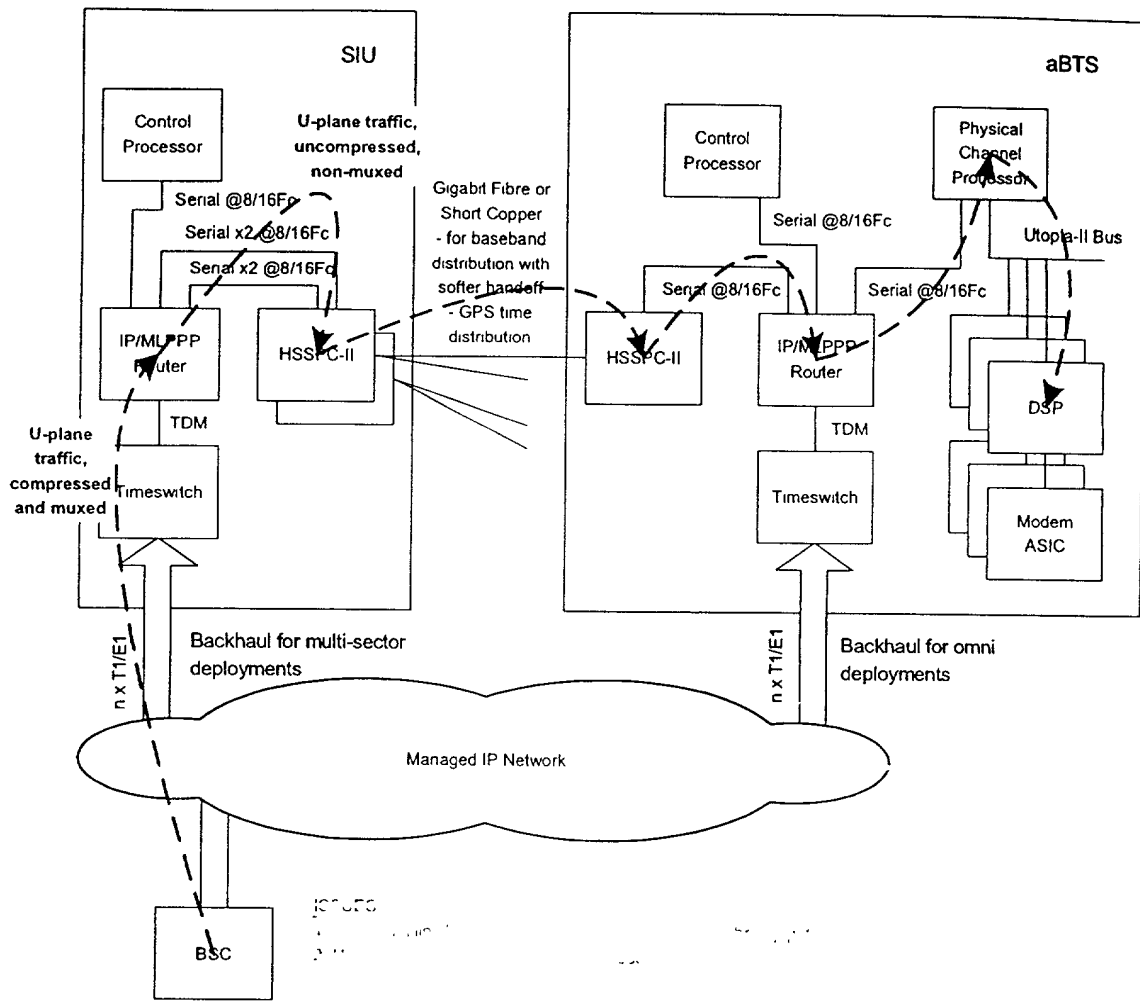


FIG. 44

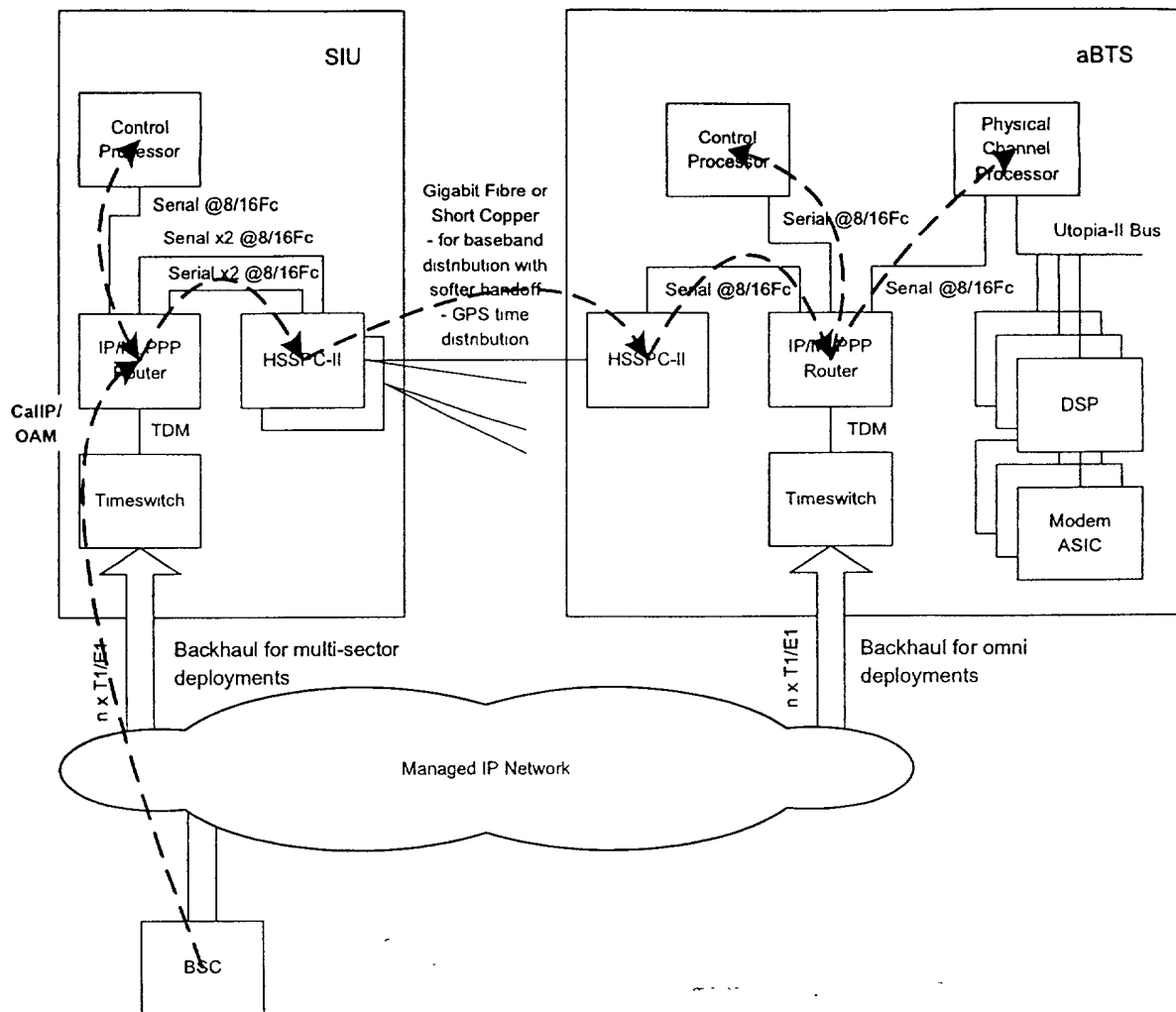


FIG. 45

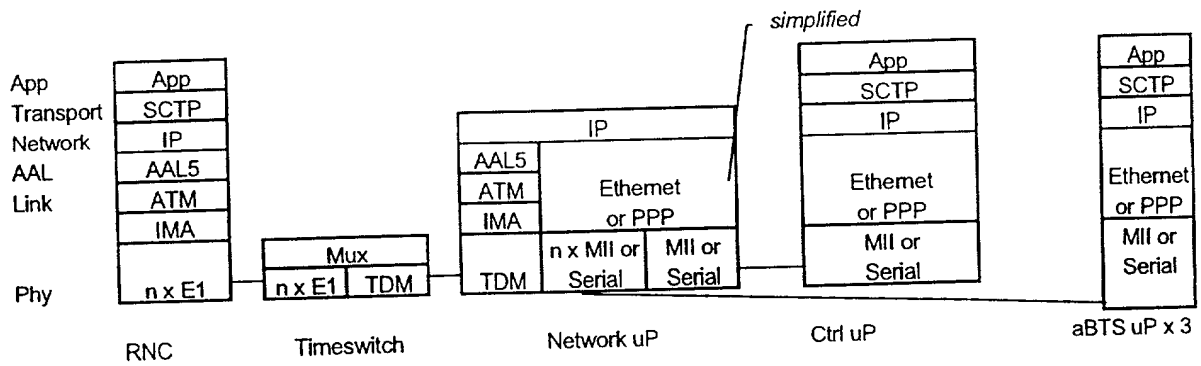


FIG. 46

UMTS '00 (IPoA backhaul) OMC-B Flow / CDMA OAM

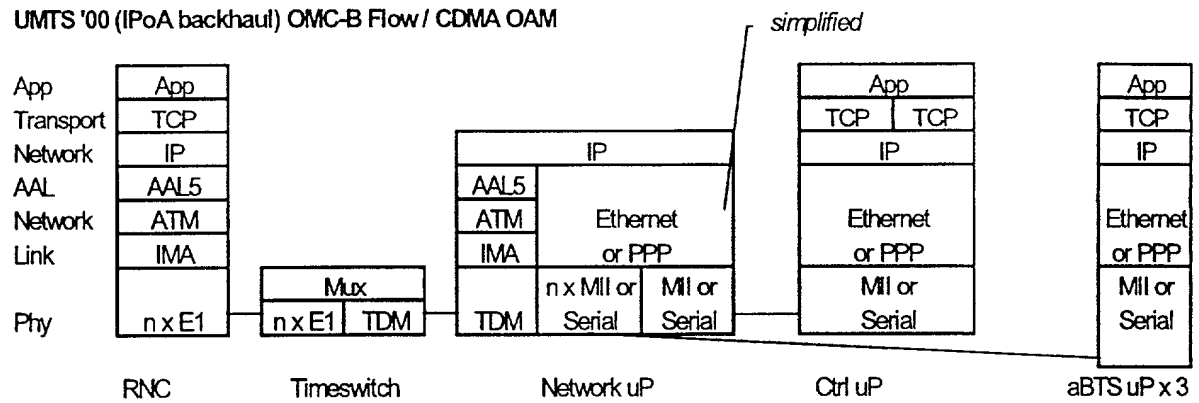


FIG. 47

UMTS '00 (IPoA backhaul) User Flow / CDMA A.bis User Traffic

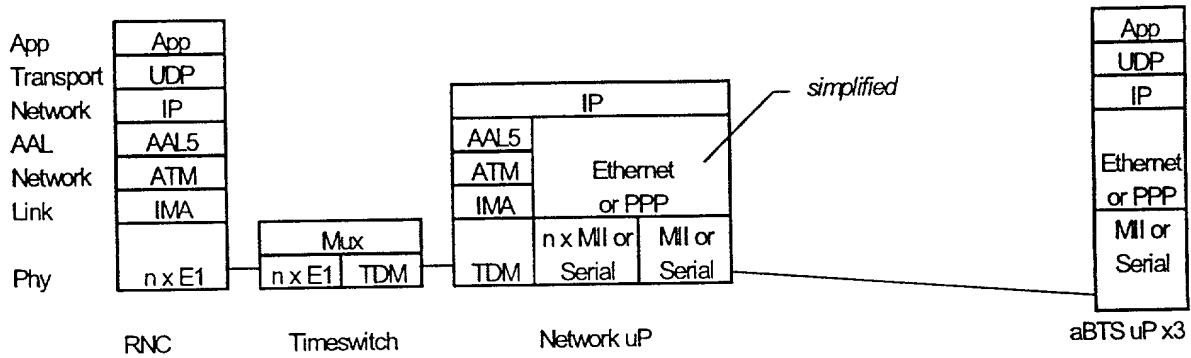


FIG. 48

FIG. 49 is a block diagram of a network architecture for multi-sector and omni deployments. The diagram shows a Managed Ethernet Network (4902) connected to a BSC (Base Station Controller) and two Base Station Units (BSUs). The BSU on the left (4906) is labeled SIU (Sector Interface Unit) and contains a Control Processor (4912), an Ethernet Switch (4910), and a 10/100 BaseTX PHY (4908). The BSU on the right (4904) is labeled aBTS (Active Base Transceiver Station) and contains a Control Processor (4914), a Physical Channel Processor (4916), an Ethernet Switch (4910), a 10/100 BaseTX PHY (4906), a DSP (Digital Signal Processor), and a Modem ASIC. The two BSUs are connected via Gigabit Fibre or Short Copper for baseband distribution with softer handoff and GPS time distribution. The Managed Ethernet Network (4902) provides backhaul for multi-sector deployments (left) and omni deployments (right).

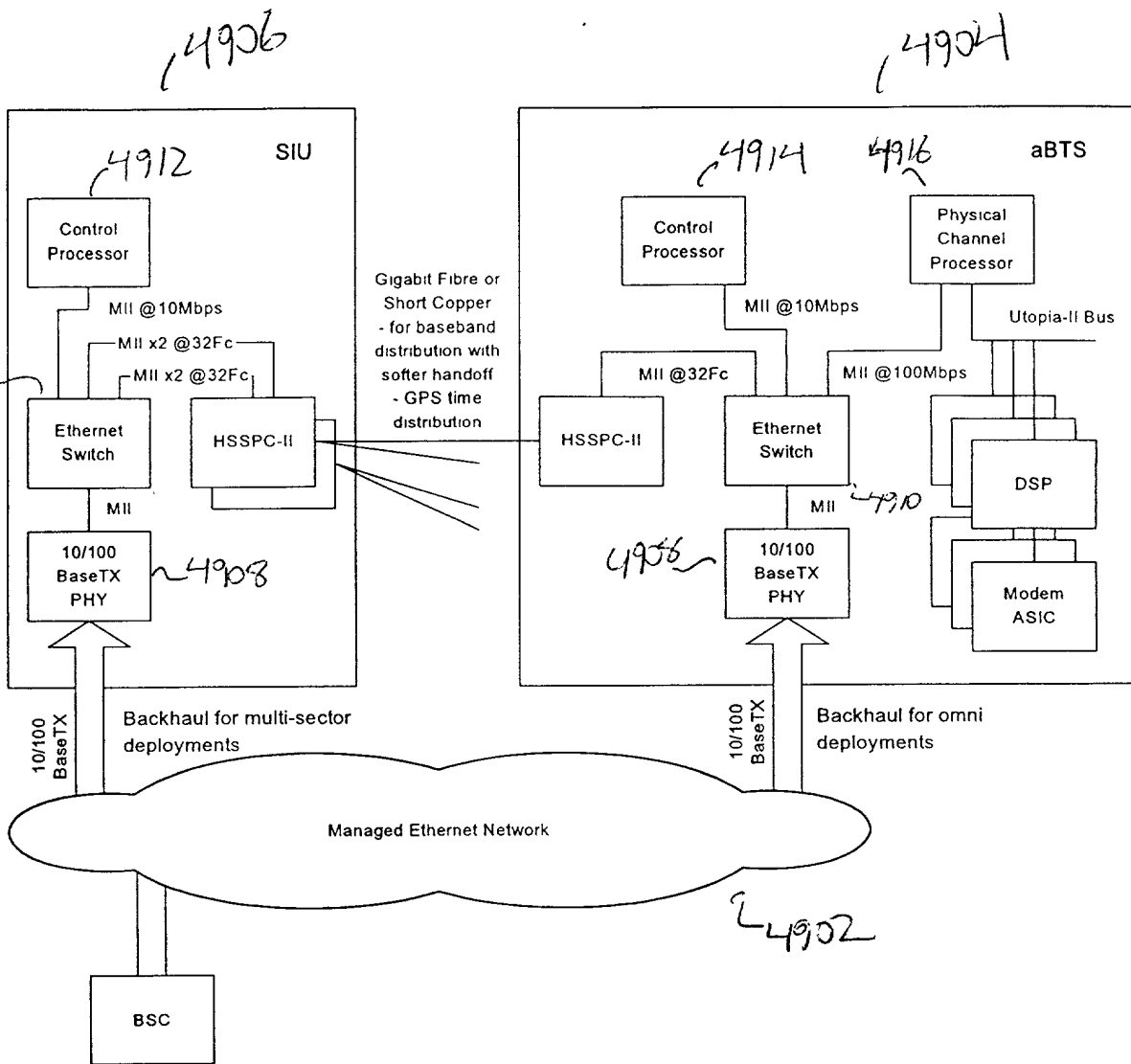


FIG. 49

UMTS '00 (IP/Ethernet backhaul) NBAP Flow / CDMA A.bis

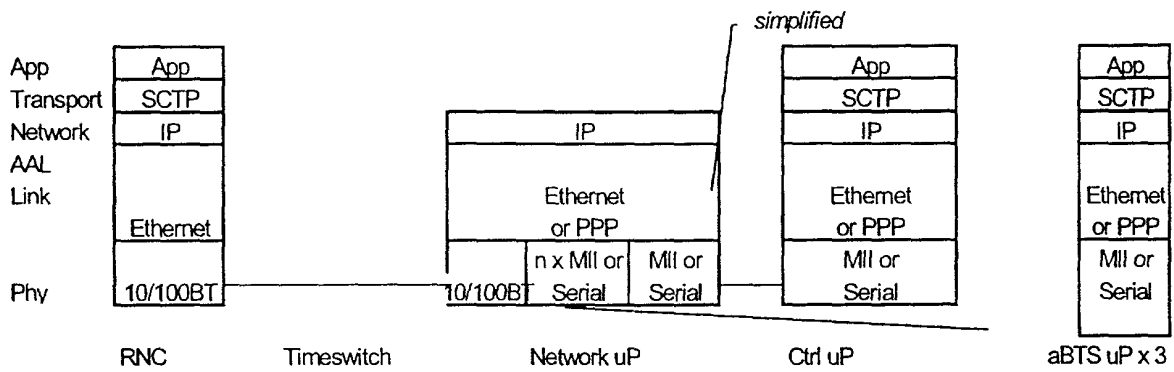


FIG. 50

UMTS '00 (IP/Ethernet backhaul) User Flow / CDMA A.bis

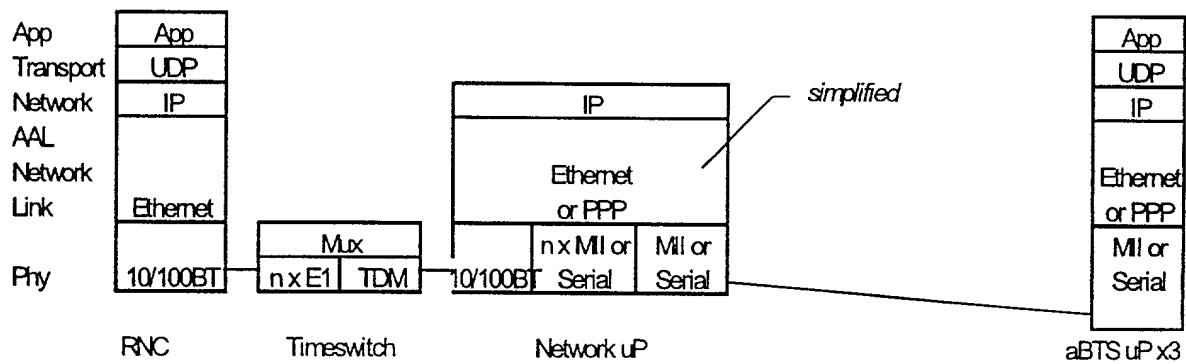


FIG. 51

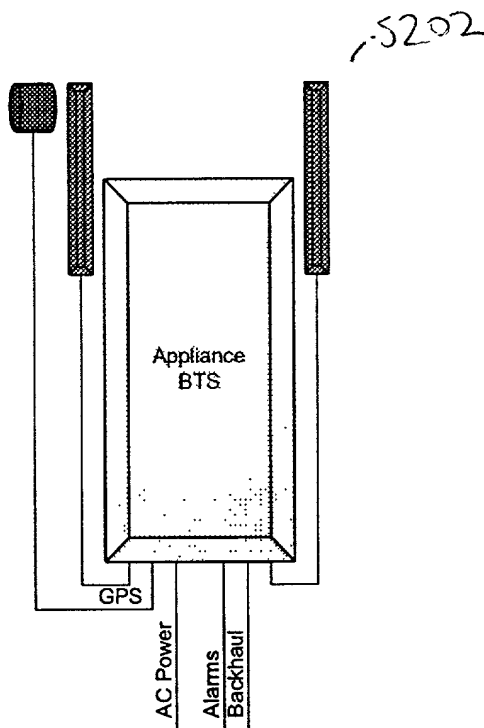


FIG. 52

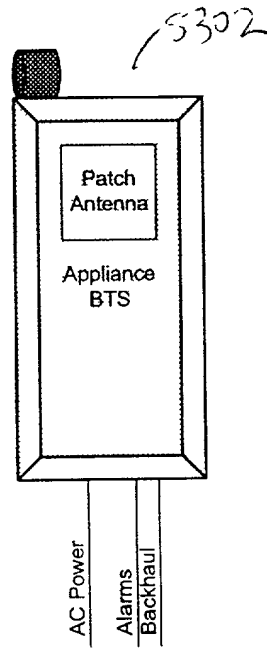


FIG. 53

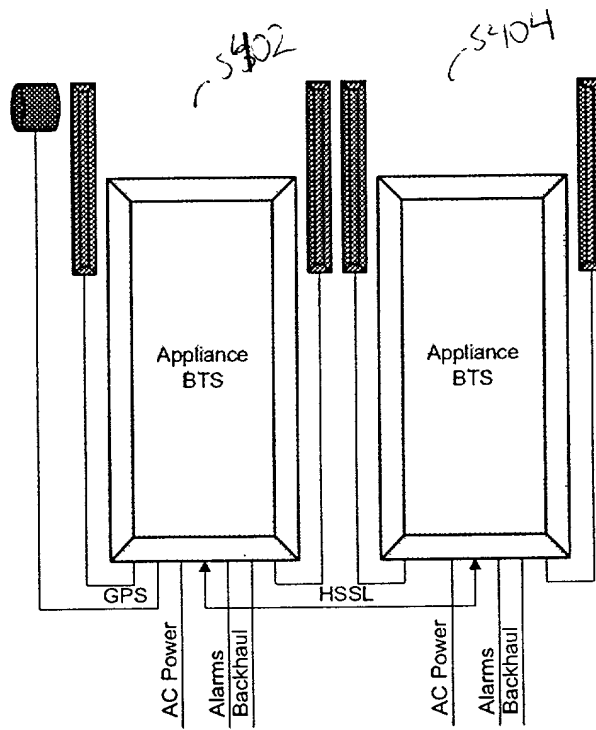


FIG. 54

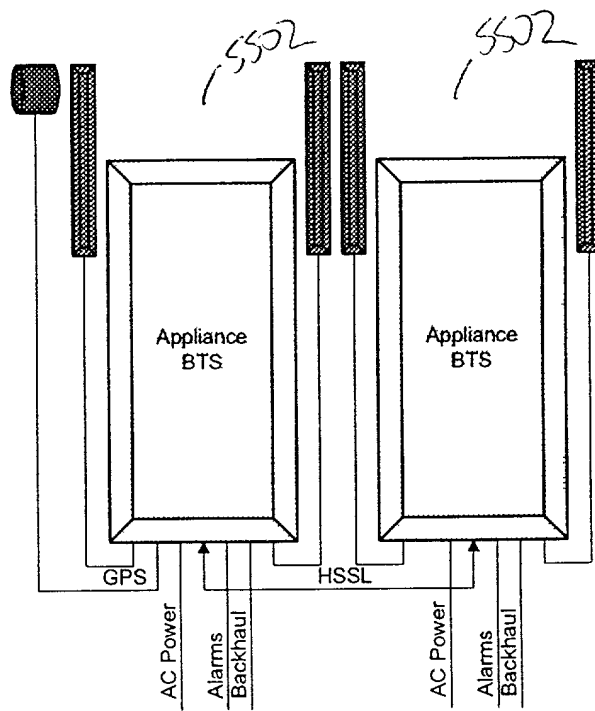


FIG. 55

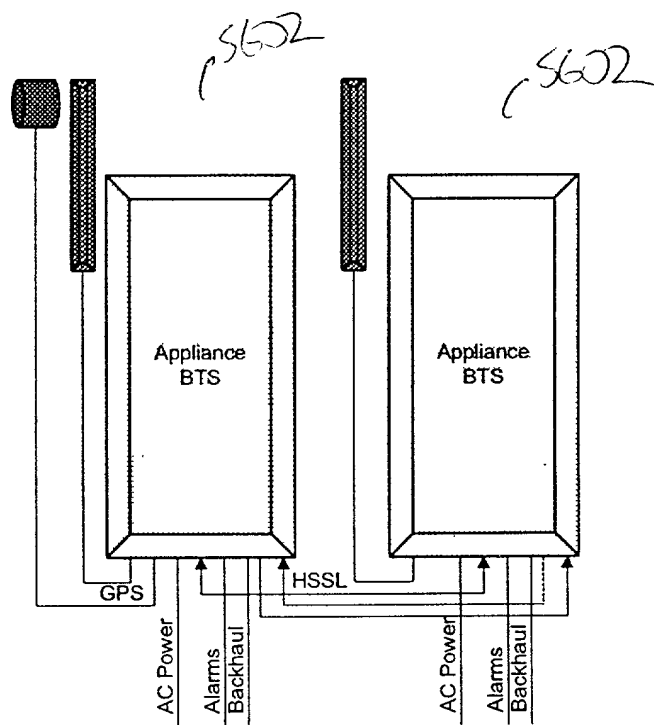


FIG. 56

5702

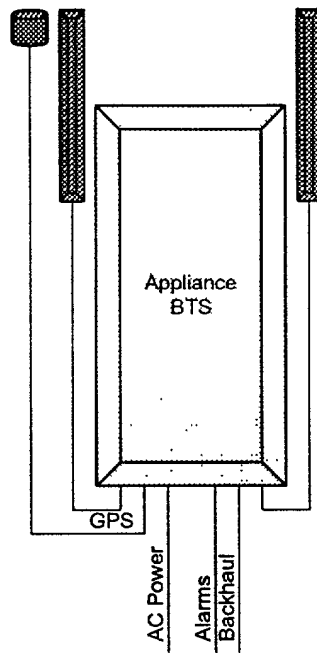


FIG. 57

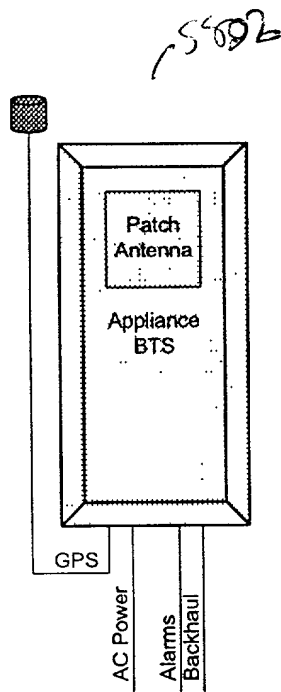


FIG. 58

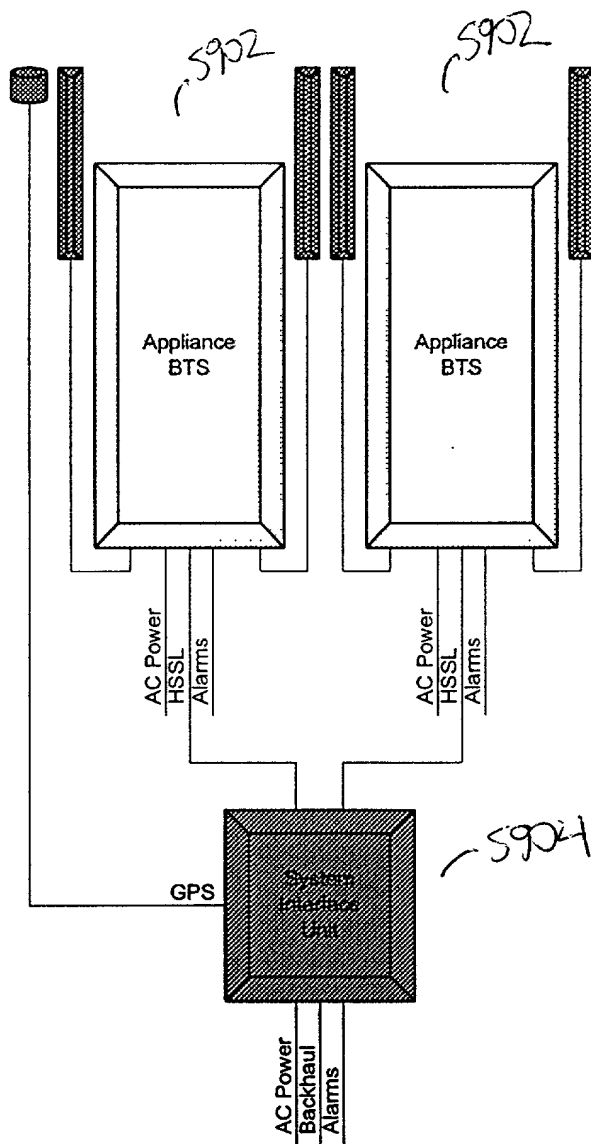


FIG. 59

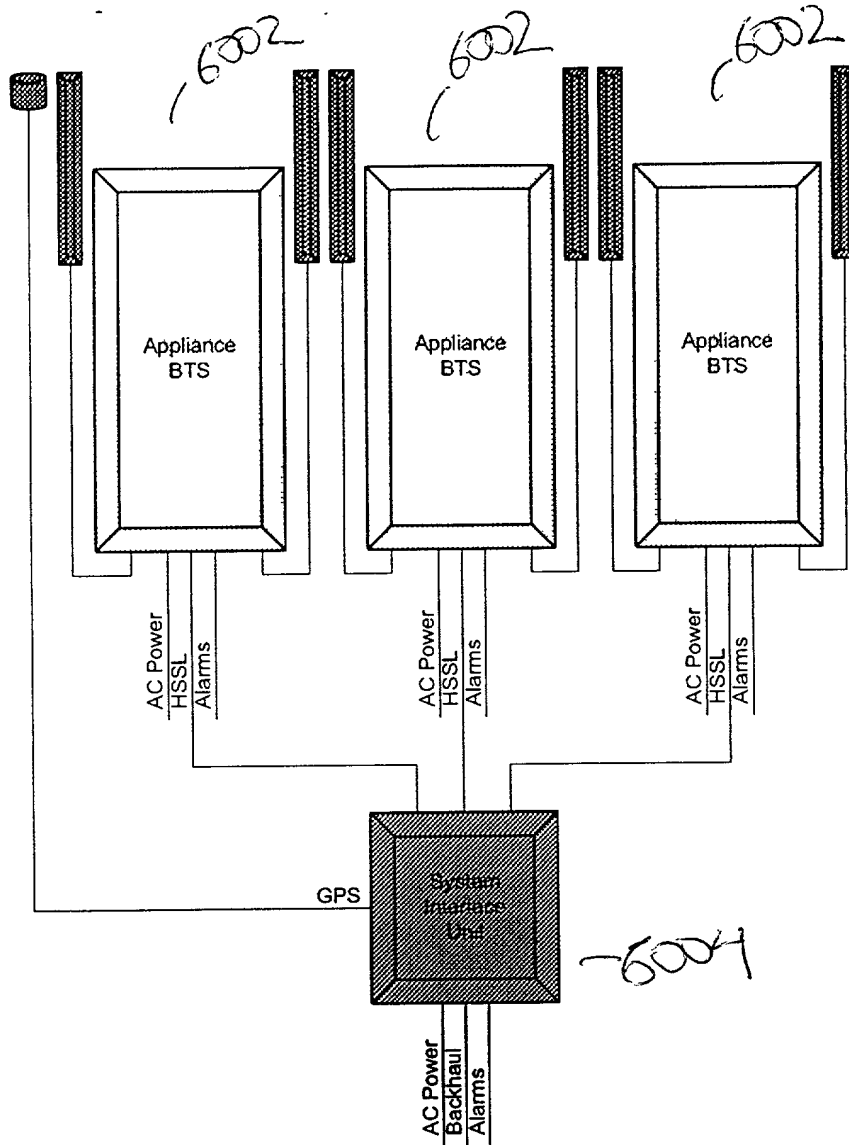


FIG. 60

6102

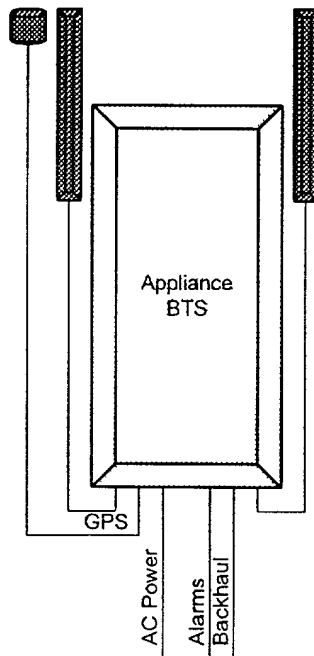


FIG. 61

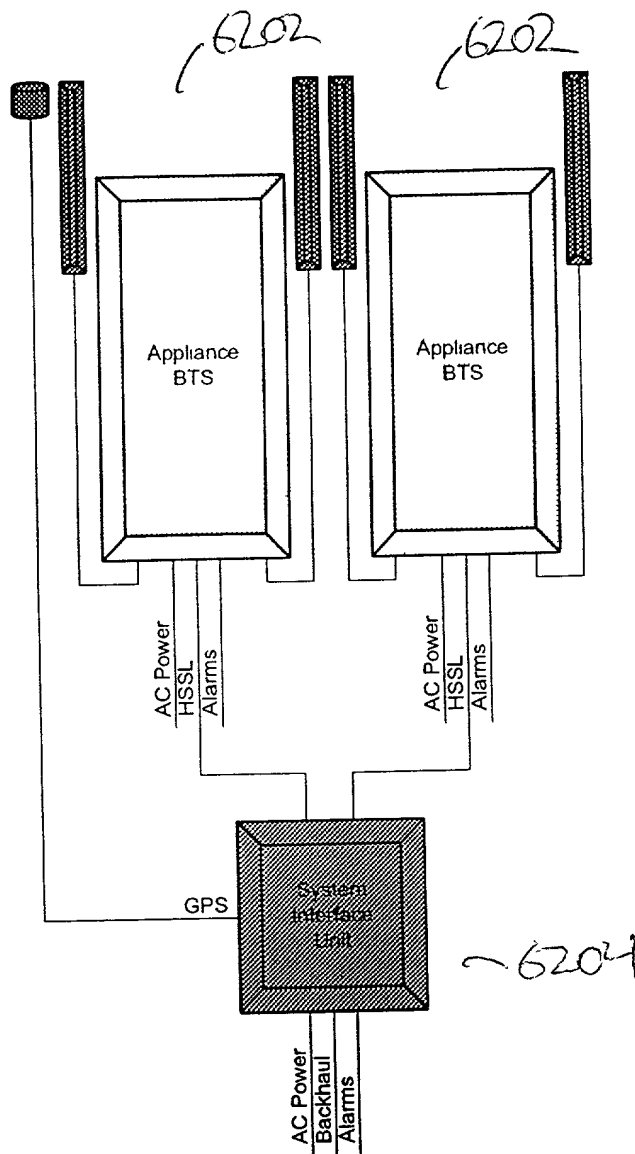


FIG. 62

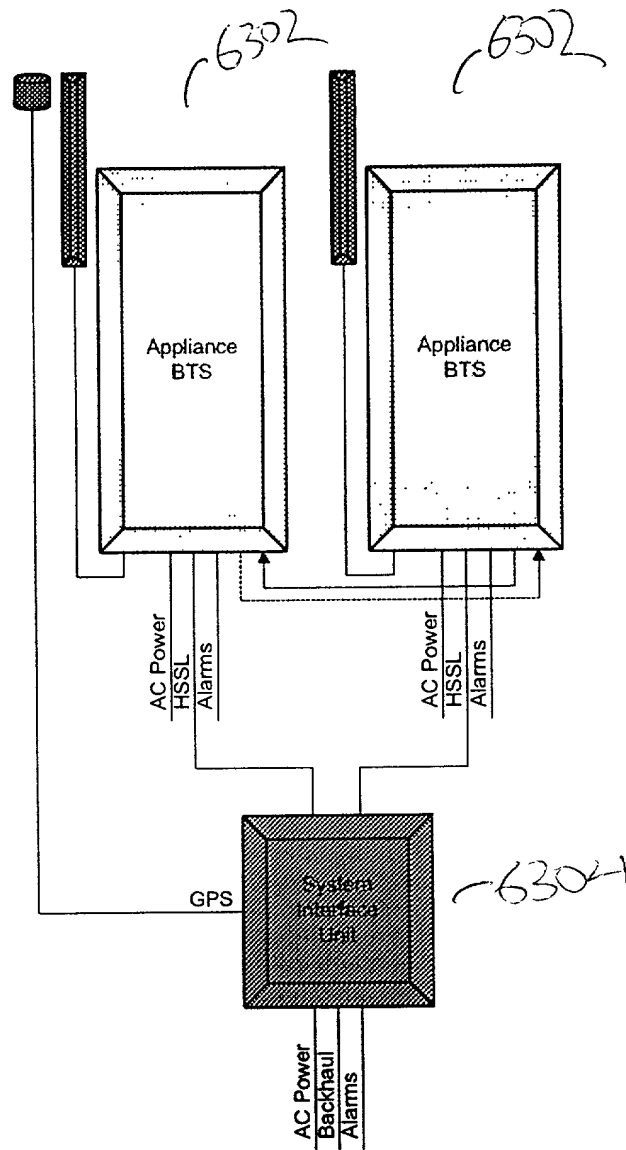


FIG. 63

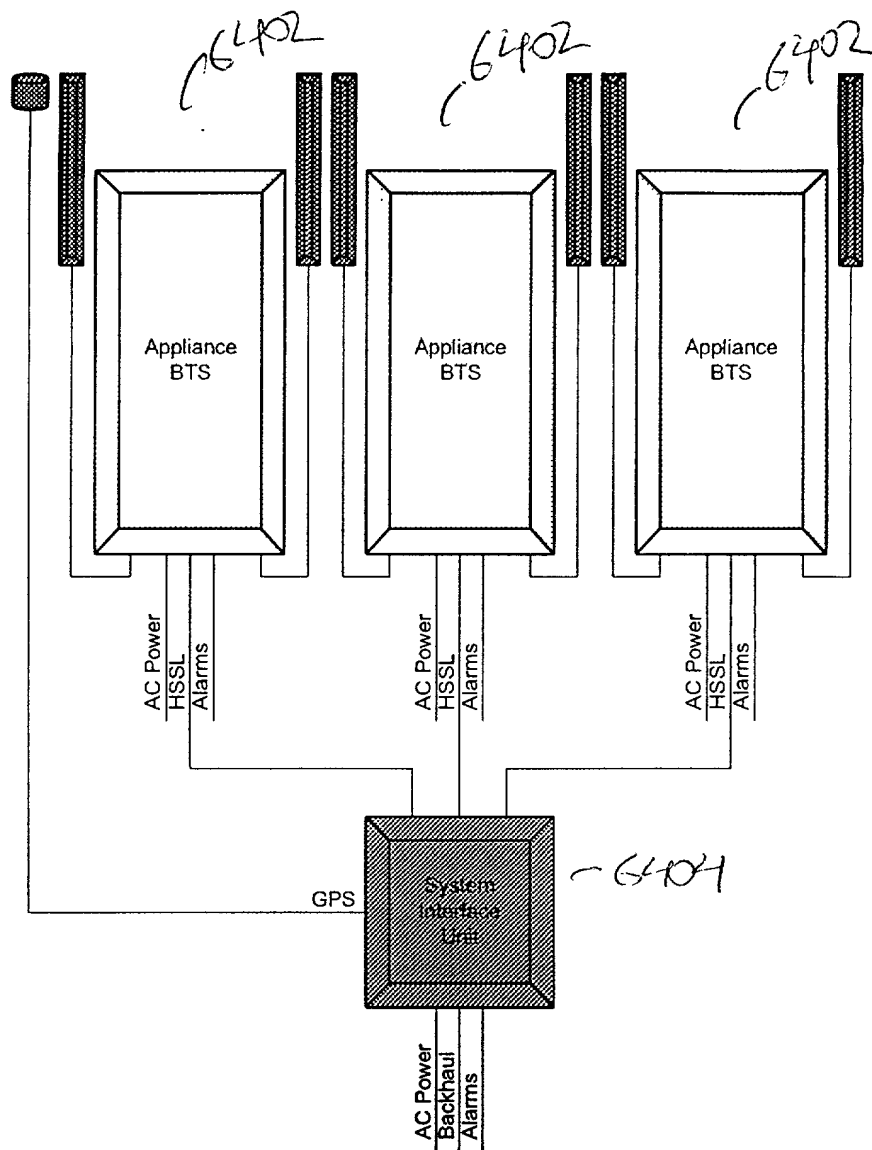


FIG. 64

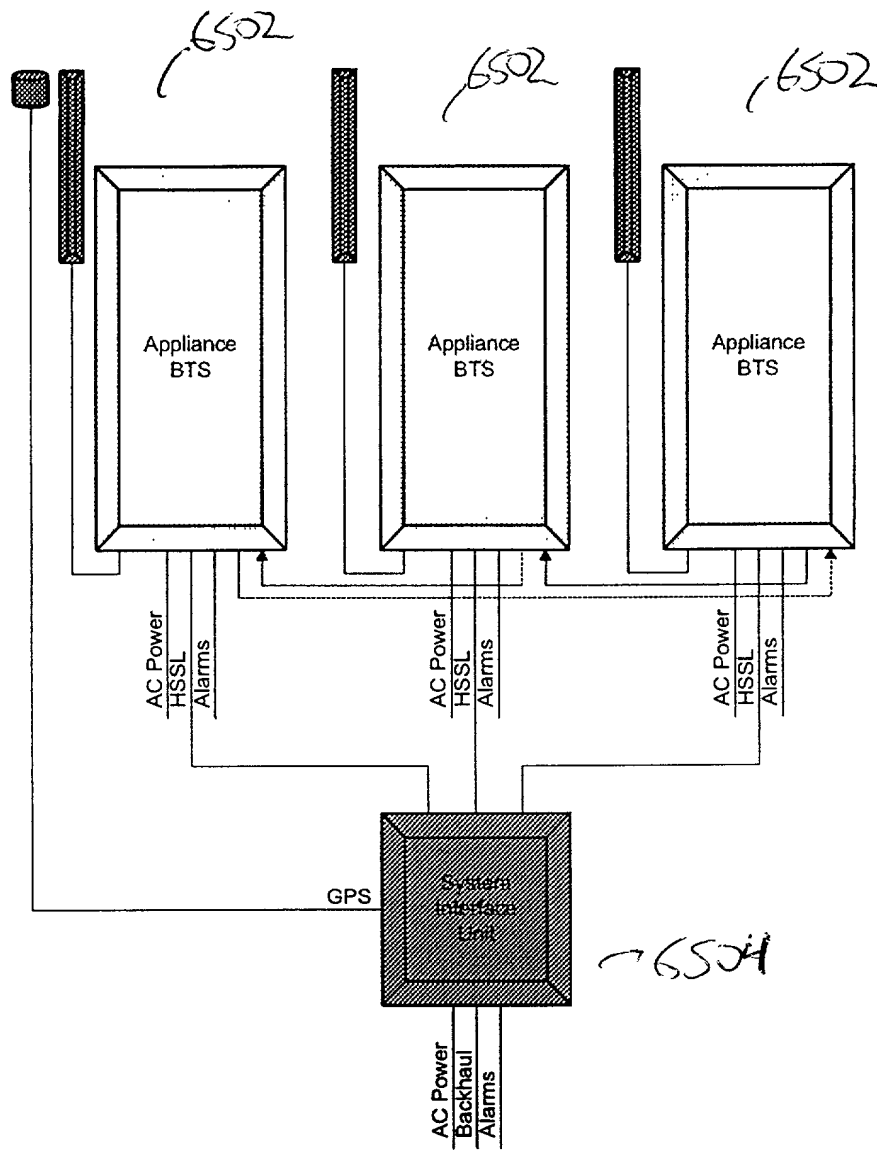


FIG. 65

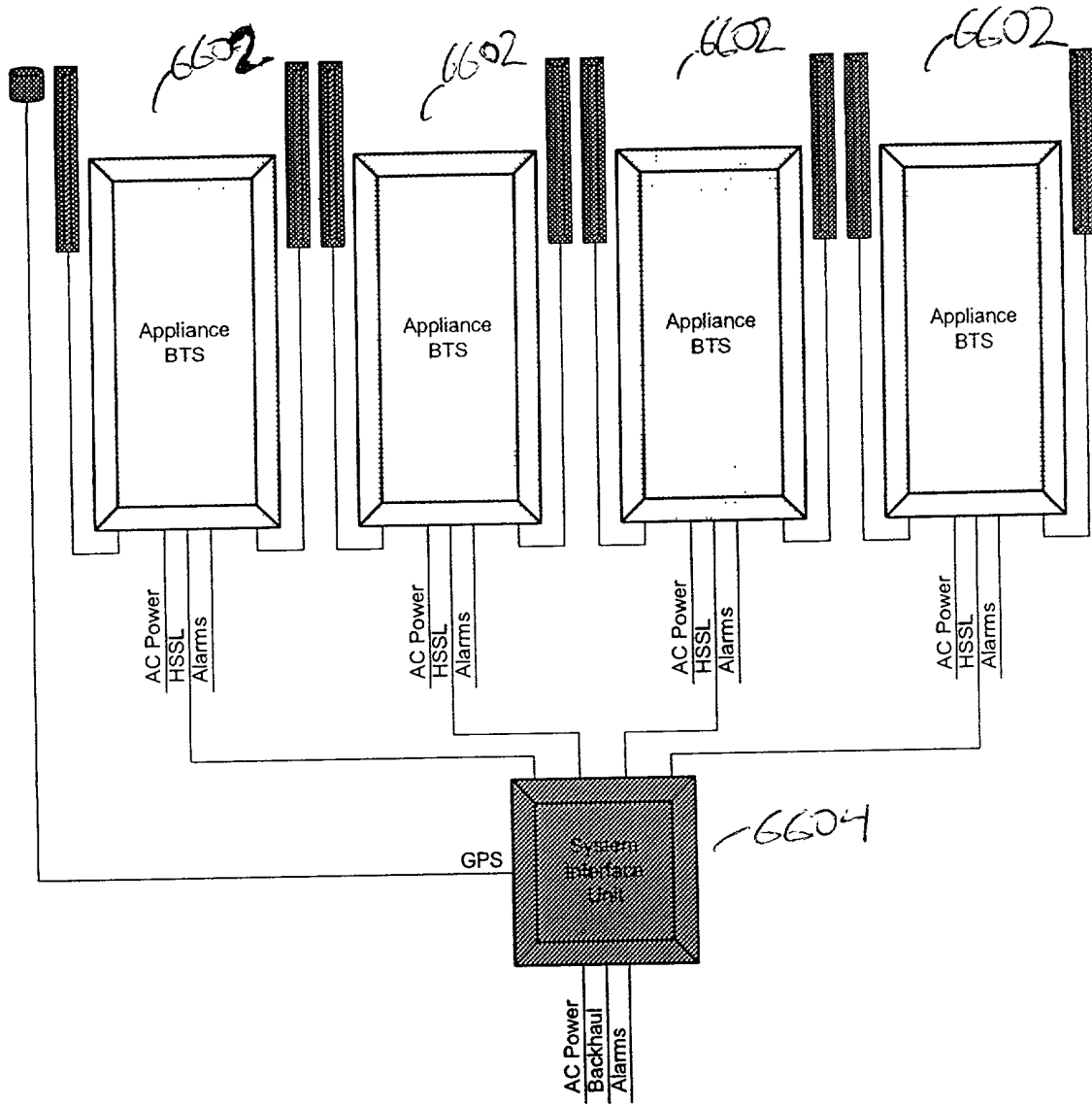


FIG.66

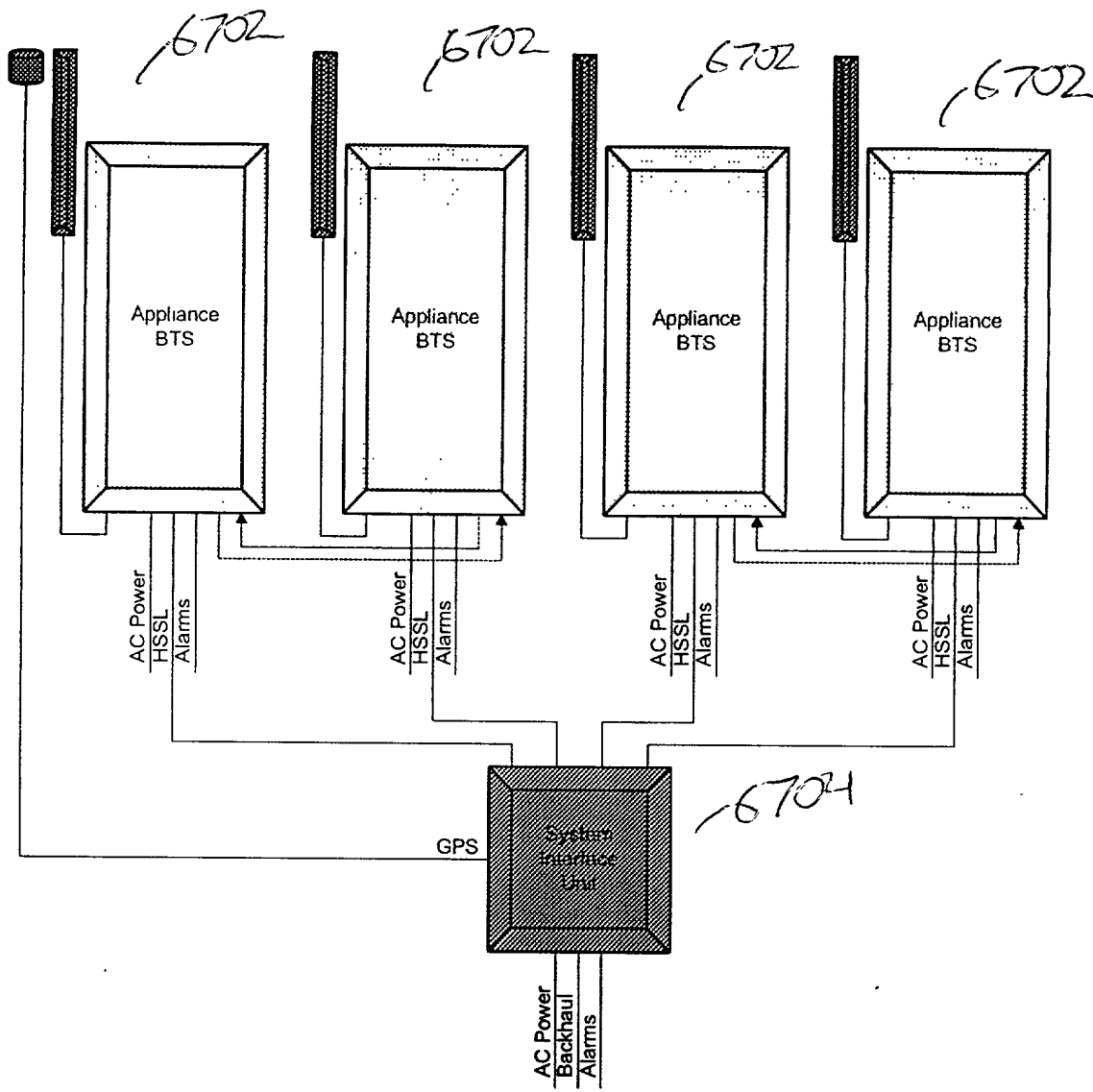


FIG. 67

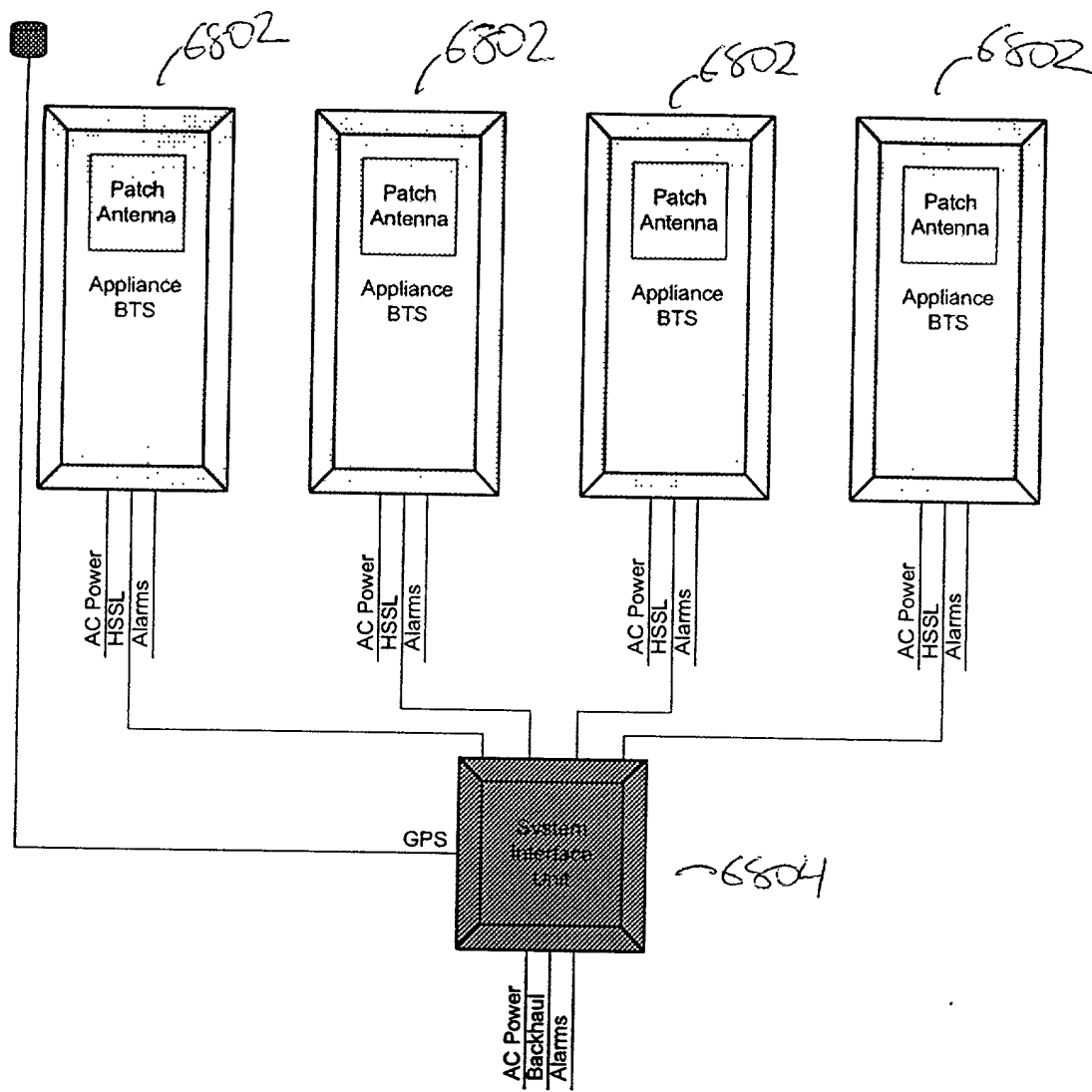


FIG. 68

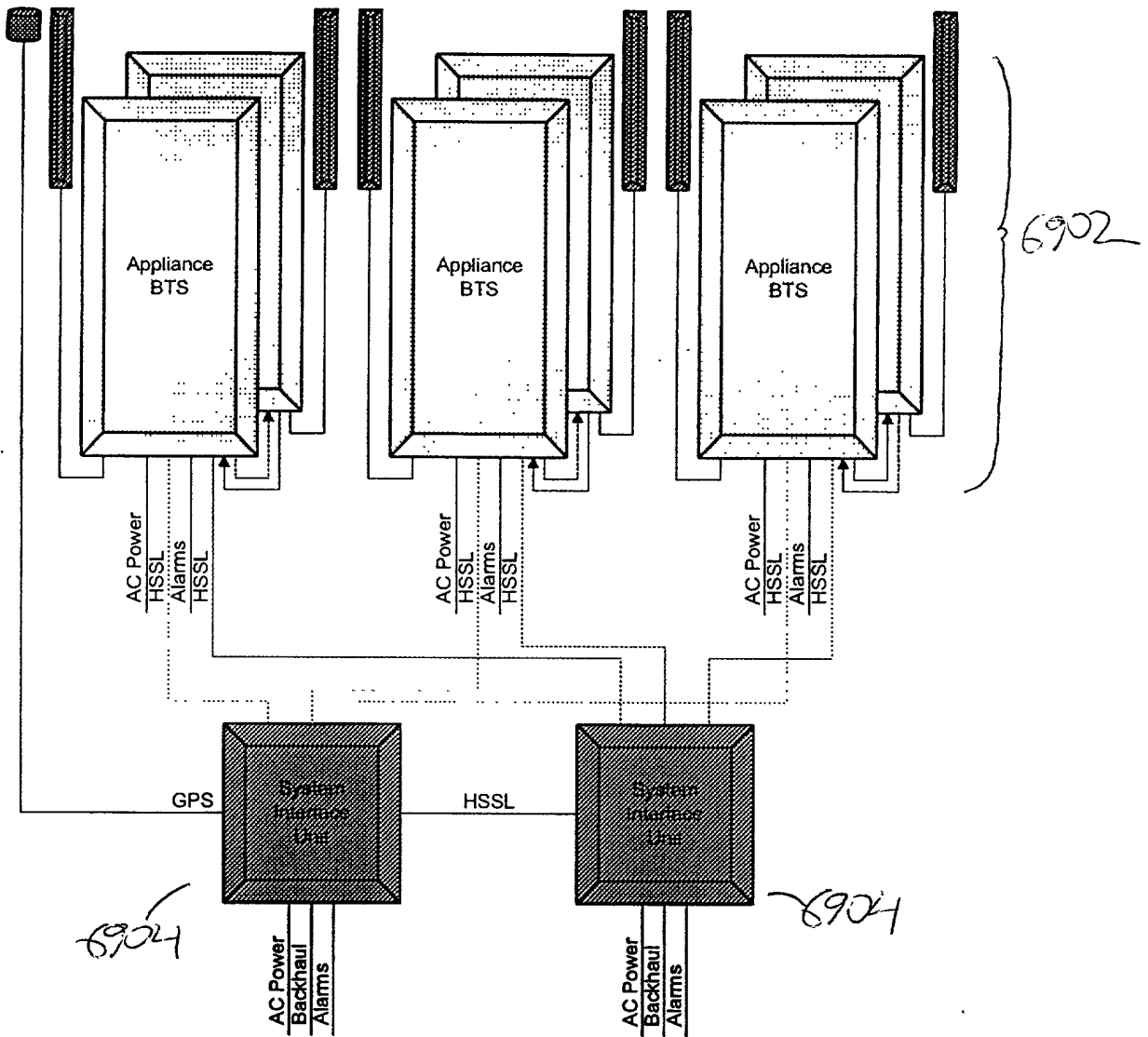


FIG. 69

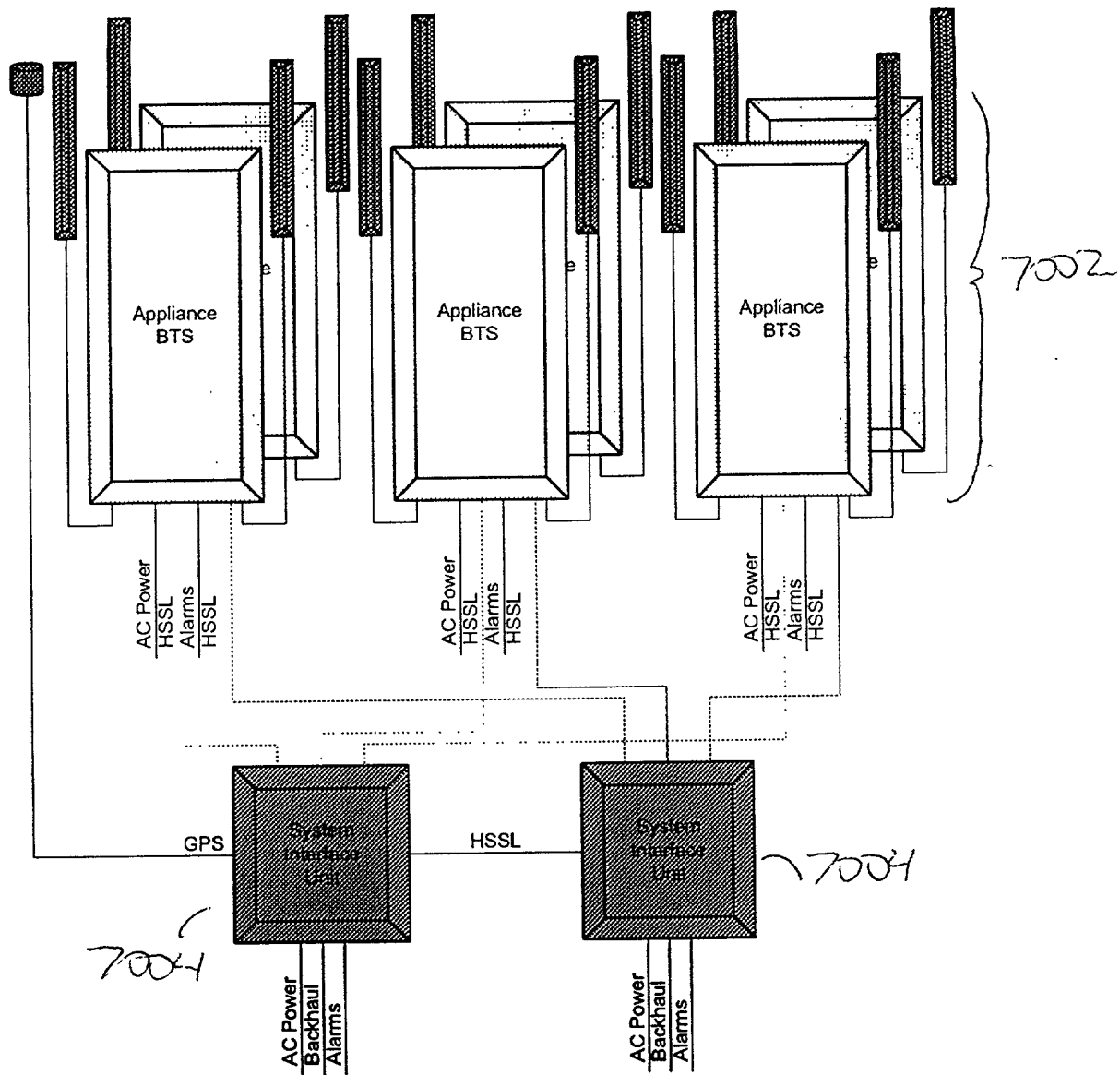


FIG. 70